Layout Note: The 0.1 µF decoupling capacitor should be placed within 100 mils from the GMCH pins.

Layout Note: The H_RCOMP trace should be 10-mil wide with 20-mil spacing.

Layout Note: H_SCOMP trace should be 100/F/04 R54/2.

Layout Note: Place the 0.1 µF decoupling capacitor within 100 mils from the GMCH pins.
Ivcc (External GFX 1.310 A, integrates 1.572 A)

IVCCSM supply current 1 channel 1.615A 2 channel 3.318A

VCC AXG +1.8VSUS_GMCH

For I(min) power if not support need to for connection to 50 power

Inside GMCH cavity.

Inside GMCH cavity for VCC AXG.

Layout Note: 370 mils from edge.

-1.05V +3V

VCC AXM NCTF 50

VCC AXM NCTF 48

VCC AXM NCTF 46

VCC AXM NCTF 44

VCC AXM NCTF 41

VCC AXM NCTF 40

VCC AXM NCTF 38

VCC AXM NCTF 37

VSS_NCTF 1

VSS_NCTF 2

VSS_NCTF 3

VSS_NCTF 6

VSS_NCTF 9

VSS_NCTF 12

VSS_NCTF 14

VSS_NCTF 15

VSS_NCTF 16

VSS_NCTF 17

VSS_NCTF 19

VSS_NCTF 21

VSS_NCTF 26

VSS_NCTF 27

VSS_NCTF 30

VSS_NCTF 31

VSS_NCTF 32

VSS_NCTF 33

VSS_NCTF 37VSS_SCB1

VSS SCB 2

VSS SCB 4

Date: Monday, March 19, 2007

Custom Crestline (VCC, NCTF)
**Strap table**

All strap are sampled with respect to the leading edge of the GMCH Power OK (PWROK) Signal

CFG[17:3] Have internal Pull-up

CFG[18:19] Have internal Pull-down

Any CFG signal strapping option not list below should be left NC Pin

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Strap description</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>CFG[2:0]</td>
<td>FSB Frequency Select</td>
<td>010 = FSB 800MHz 011 = FSB 667MHz</td>
</tr>
<tr>
<td>CFG[4:3]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>CFG5</td>
<td>DMI X2 Select</td>
<td>0 = DMI X2 1 = DMI X4(Default)</td>
</tr>
<tr>
<td>CFG6</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>CFG7</td>
<td>CPU Strap</td>
<td>0 = Reserved 1 = Mobile CPU(Default)</td>
</tr>
<tr>
<td>CFG8</td>
<td>Low power PCI Express</td>
<td>0 = Normal mode 1 = Low Power mode</td>
</tr>
<tr>
<td>CFG9</td>
<td>PCI Express Graphics Lane Reversal</td>
<td>0 = Reverse Lanes 1 = Normal operation(Default)</td>
</tr>
<tr>
<td>CFG[11:10]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>CFG[13:12]</td>
<td>XOR/ALLZ</td>
<td>00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)</td>
</tr>
<tr>
<td>CFG15:14</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>CFG16</td>
<td>FSB Dynamic OGT</td>
<td>0 = Dynamic OGT disable 1 = Dynamic OGT Enable(Default)</td>
</tr>
<tr>
<td>CFG[18:17]</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>SDVO_CTRLDATA</td>
<td>SDVO Present</td>
<td>0 = No SDVO Card present(Default) 1 = SDVO Card Present</td>
</tr>
<tr>
<td>CFG19</td>
<td>DMI Lane Reversal</td>
<td>0 = Normal operation 1 = Reverse Lanes</td>
</tr>
<tr>
<td>CFG20</td>
<td>SDVO/PCIe concurrent</td>
<td>0 = Only SDVO or PCIe x1 is operation(Default) 1 = SDVO and PCIe x1 are operating simultaneously via the PEG port</td>
</tr>
</tbody>
</table>

**DSI X2 Select**

<table>
<thead>
<tr>
<th>Configuration</th>
<th>MCH_CFG_5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low = DMIX2</td>
<td>High = DMIX4(Default)</td>
</tr>
</tbody>
</table>

**DMI Lane Reversal**

<table>
<thead>
<tr>
<th>Configuration</th>
<th>MCH_CFG_10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low = Normal operation(Default)</td>
<td>High = Reverse Lane</td>
</tr>
</tbody>
</table>

**XOR/ALLZ/Clock Un-gating**

<table>
<thead>
<tr>
<th>Configuration</th>
<th>MCH_CFG_11</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 = XOR Mode Enable</td>
<td>1 = All-Z Mode Enable</td>
</tr>
<tr>
<td>1 = Normal operation(Default)</td>
<td></td>
</tr>
</tbody>
</table>

**PCI Express Graphics**

<table>
<thead>
<tr>
<th>Configuration</th>
<th>MCH_CFG_12</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low = Reverse Lane</td>
<td>High = Normal operation(Default)</td>
</tr>
</tbody>
</table>

**SDVO Present**

Strap define at External DVI control page
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

DDRII B CHANNEL

Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

Uninstall

SI-1 modify (add terminator resistor)
Place these Caps near So-Dimm1.

Place these Caps near So-Dimm2.

No Vias Between the Trace of PIN to CAP.

No Vias Between the Trace of PIN to CAP.

Place these Caps near So-Dimm1.

Place these Caps near So-Dimm2.

No Vias Between the Trace of PIN to CAP.

No Vias Between the Trace of PIN to CAP.
close conn within 600mils

CRT SWITCH

SI-1 modified for fix CRT

rise time issue

filter for HDTV

SI-1 MODIFY

EMI

CRT SWITCH

SI-1 modified for fix CRT

rise time issue

inputs  function

/E SET

L  L  V = port 0

L  H  V = port 1

H  X  Disconnect

PROJECT : AT5
Quanta Computer Inc.
0312 Gain Table

<table>
<thead>
<tr>
<th>GAIN</th>
<th>GAIN 1 SE(BTL AVINV)</th>
<th>0</th>
<th>0</th>
<th>6dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>GAIN</td>
<td>GAIN 1 SE(BNL AVINV)</td>
<td>1</td>
<td>1</td>
<td>15.6dB</td>
</tr>
<tr>
<td>GAIN</td>
<td>GAIN 1 SE(BNL AVINV)</td>
<td>x</td>
<td>x</td>
<td>6.1dB</td>
</tr>
</tbody>
</table>

PCPK BEEP

LINE OUT Amplifier

Note: The document contains a schematic diagram of an audio amplifier circuit, including gain settings, component values, and connections. The text includes gain settings for different configurations, and notes on changes to the component footprint and EMI requests.

---

SI-2 remove R739, R731 from realtek request for fix BO voice when audio jack unplugs.

SI-1 ADD EMI request.

SI-1 ADD EMI request.

SI-1 ADD EMI request.
R21 value should be 2.49k (1%) for 8111B/8111C application. R21 should be 2.9k(1%) for 8101E application.

BLOCK A is only for RTL8101E application.
Power domain chart

<table>
<thead>
<tr>
<th>Power Domain</th>
<th>RTL8111B / RTL8101E</th>
</tr>
</thead>
<tbody>
<tr>
<td>LANVCC</td>
<td>3.3V</td>
</tr>
<tr>
<td>LAN_D1.8</td>
<td>1.8V</td>
</tr>
<tr>
<td>LAN_A1.8</td>
<td>1.8V</td>
</tr>
<tr>
<td>LAN_D1.5</td>
<td>1.5V</td>
</tr>
</tbody>
</table>

Q1 | Q3
---|---
RTL811B | Need | Need |
RTL8101E | N/A | N/A |
C30: Add PD22 for 12-cell battery issue
Vout = (1 + Ra/Rb) * Vout

Rc = [1 + (Rc/Rd)] * Vout

FSET = GND = 200KHz
REF f = 300KHz
VCC f = 500KHz

Peak current: 8.5A
Continue current: 6.5A

OCP minimum 10A
+1.5 Volt +/- 5%

OCP minimum 20A
+1.05 Volt +/- 5%

Peak current: 16A
Continue current: 13A

-1.5V & VCCP +1.05V (MAX8743)

+1.05 Volt +/- 5%
Peak current: 16A
OCF minimum 20A

+1.5 Volt +/- 5%
Countinue current: 6.5A

-26x368 [+1.5V] 3,4,10,22,24,35,38,39,45,46

42
Sense lines are 18 mil wide, 2Ω=37.4 Ohm.
Use differential routing with 7 mil spacing.
Route external layer with solid GND reference (no split planes).
Use 25 mil separation from any other signal.

Add layout note on pins 22 and 28 of MAX8771 controller. These nets have large voltage swings.
Needed to route them away from the sensitive areas that are trying to detect small changes in voltage, such as the voltage sense VchAss, VchSens, and lines.

*Use 25 mil separation from any other signal.*
1.1 Volt +/- 5%
Countinue current: 11A
Peak current: 13.5A
OCP minimum 17A

to external
VGA core
power
(16.25A)

Max Current? A

Vout1=(1+R1/R2) * 0.5

Vcs=I_L(A)*L_DCR(mOHM)=V_ILIM(mV)/10

HI
LO

NVIDIA
G3

V_PWRCNTL

TON=REF, F= 450KHz
TON=OPEN, F= 300KHz

4.2mOHM

Current limit =:17A

OCP minimum 17A

1.1 Volt +/- 5%

Peak current: 13.5A

Countinue current: 11A

OCP minimum 17A

For Discrete Only
1.8 Volt +/- 5%
Countinue current: 12A
Peak current: 15A
OCP minimum 18A

\[ V_O = \frac{0.8(R_1+R_2)}{R_2} \]

R_2 < 120Kohm

OCP minimum 18A
1.8 Volt +/- 5%
Peak current: 15A
Continue current: 12A

For Discrete Only

For G734GVX VGA
PLL power

for G734GVX VGA
memory bus power