The naming rule is value + R + size + tolerance

For the value, it can be read by the number before R. (R means resistor)

For the tolerance, it can be read from the last letter.
CK410# = 0, CK410 MODE
CK410# = 1, CK409 MODE

CLOCK FREQUENCY SELECT TABLE (MHz)

<table>
<thead>
<tr>
<th>FSC</th>
<th>FSB</th>
<th>FSA</th>
<th>CPU</th>
<th>SRC</th>
<th>PCI</th>
<th>REF</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 1</td>
<td>133</td>
<td>100</td>
<td>100</td>
<td>33</td>
<td>4.31</td>
<td></td>
</tr>
<tr>
<td>0 1 1</td>
<td>166</td>
<td>100</td>
<td>100</td>
<td>33</td>
<td>4.31</td>
<td></td>
</tr>
<tr>
<td>0 1 0</td>
<td>200</td>
<td>100</td>
<td>100</td>
<td>33</td>
<td>4.31</td>
<td></td>
</tr>
<tr>
<td>0 0 0</td>
<td>250</td>
<td>100</td>
<td>100</td>
<td>33</td>
<td>4.31</td>
<td></td>
</tr>
<tr>
<td>1 0 0</td>
<td>333</td>
<td>100</td>
<td>100</td>
<td>33</td>
<td>4.31</td>
<td></td>
</tr>
<tr>
<td>1 1 0</td>
<td>400</td>
<td>100</td>
<td>100</td>
<td>33</td>
<td>4.31</td>
<td></td>
</tr>
<tr>
<td>1 1 1</td>
<td>RESV</td>
<td>100</td>
<td>100</td>
<td>33</td>
<td>4.31</td>
<td></td>
</tr>
</tbody>
</table>

For Yonah Cerlon-M
For Yonah Cerlon-M
NB Strap pins

All pull-up and pull-down resistors are 4.7kohm.

Select the FSB SPEED

<table>
<thead>
<tr>
<th>BMREQ</th>
<th>HSYNC</th>
<th>VSYNC</th>
<th>Freq.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>100MHZ</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>333MHZ</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>166MHZ</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>100MHZ</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>100MHZ</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>100MHZ</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>-------</td>
</tr>
</tbody>
</table>

BMREQ is pulled down if CPU doesn't support BSEL2.

Adjust PCI-E Amp. R->Small then Amp->Large
**PARALLEL TERMINATION**

Put decap near power (0.9V) and pull-up resistor

**Decoupling Capacitor**

Put decap near power (0.9V) and pull-up resistor

Place these Caps near DM1

Place these Caps near DM2
**Ferrite bead impedance:** 30 ohms @ 180MHz.

**Layout Note:**
- Must be a ground return path between this ground and the ground on the VGA connector.
- Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT_CONN. RGB will hit 75 Ohm first, pi-filter, then CRT_CONN.

---

**CRT I/F & CONNECTOR**

**Hsync & Vsync level shift**

**DDC_CLK & DATA level shift**

PH at RC410ME side

**TV OUT CONN**

*Must be a ground return path between this ground and the ground on the VGA connector.*
When no SATA replace to 0 ohm.
3D3V_S0 must never exceed V5_VREF by more than 0.6V.

Vf = 0.38v (81nA)
1v (840nA)

3D3V_S0 must never exceed V5_VREF by more than 0.6V.

1D8V_S0 must never exceed 3D3V_S0 by more than 0.6V.
1D8V_S0 must start ramping up within 1ms of 3D3V_S0 starting to ramp p.
REQUIRED STRAPS

CPU F=K8

ROM TYPE:
H, H = PCI ROM
L, H = LPC I ROM
L, L = LPC ROM
L, L = FWH ROM
NOTE: FOR SB460, PCI_CLK[8:7] ARE DEFAULT CONNECTED TO SUBSTRATE BALLS PCI_CLK[1:0]

LFRAME#

RTC_IRQ#15

RTC_CLK15,20

SB_CLK33_LAN15,23

SB_CLK33_MINI15,32

SB_CLK33_FWH15,36

LPC_LFRAME#15,33,35,36

USB wake from S5 supported.

DEBUG STRAPS

IDE_DACK#

IDE_PLL
PULL HIGH
USE LONG RESET DEFAULT
BYPASS PCI PLL
BYPASS ACPI BCLK
BYPASS IDE PLL
USE EEPROM PCIE STRAPS

PULL LOW
USE SHORT RESET DEFAULT
USE PCI PLL DEFAULT
USE ACPI BCLK DEFAULT
USE IDE PLL DEFAULT
USE DEFAULT PCIE STRAPS DEFAULT
NOTE: FOR SB460, PCI_AD23 IS RESERVED
SB460 ONLY
SB600 ONLY
SB600 ONLY

RTC_DOUT

AC97_DOUT

RTC_CLK

SB600 ONLY

USB PHY POWERDOWN DISABLE DEFAULT
ENABLE THERMTRIP DEFAULT

PCI_CLK0

PCI_CLK1

PCI_CLK2

PCI_CLK3

PCI_CLK4

PCI_CLK5

PCI_CLK6

PCI_CLK7

ACPWRO

SPDIF_OUT

PCI_CLK2

PCI_CLK3

PCI_CLK4

PCI_CLK5

PCI_CLK6

LFRAME#

SB460 ONLY
SB460 ONLY
SB600 ONLY
SB600 ONLY
LAN Connector

1. Route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias. No 90 degree bends.
4. PAIRS MUST BE EQUAL LENGTHS.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ45 moat.
8. RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP, DOC_RING, TIP, RING:
WIS: 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer: RJ45 PIN

<table>
<thead>
<tr>
<th>TD+</th>
<th>TD-</th>
<th>RD+</th>
<th>RD-</th>
<th>RX+</th>
<th>RX-</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX+</td>
<td>TX-</td>
<td>RX+</td>
<td>RX-</td>
<td>TX+</td>
<td>TX-</td>
</tr>
<tr>
<td>TD+</td>
<td>TD-</td>
<td>RD+</td>
<td>RD-</td>
<td>RX+</td>
<td>RX-</td>
</tr>
</tbody>
</table>
Mini Card Connector

UIM

Place near MINIC1

Internal Microphone

2nd source: 62.10043.331

2nd source: 20.89436.002
Add 0.01uF for TQFP

SB

R5C832_1394_7IN1(1/2)

1394 : INTAE
6IN1 : INTB(CTRL_PIN)# select

GNT : PCI_GNTW3
REQ : PCI_REQW3

SB Modify

PC/BE0#[45..22..0]

GBUS_GRST#

PCLK_R5C832_1394_7IN1(1/2)

PM_CLKRUN#15,32,33,35

<Variant Name>

<Variant Name>

<Variant Name>

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www.kyhuavitinh.com
1) When GPIO0 is asserted, AMP should be muted.
2) SPDIFO should be turned off when not used.

Configuration:
(3 External Jacks, 1 internal Mic, 1 stereo output speaker Amp.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Location</th>
<th>Re-tasking</th>
</tr>
</thead>
<tbody>
<tr>
<td>35/36</td>
<td>FRONT</td>
<td>AMP, Jack1</td>
<td>AMP output, line input</td>
</tr>
<tr>
<td>39/41</td>
<td>SURR</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>43/44</td>
<td>CEN/LEFT</td>
<td>X</td>
<td>Surr-vrefo-L/R</td>
</tr>
<tr>
<td>45/46</td>
<td>SIDESURR</td>
<td>X</td>
<td>Sidesurr-L is mic2-vrefo-R, sidesurr-R is Line2-vrefo-R</td>
</tr>
<tr>
<td>23/24</td>
<td>LINE1</td>
<td>Jack 2</td>
<td>Line input, line output</td>
</tr>
<tr>
<td>21/22</td>
<td>MIC1</td>
<td>Jack 3</td>
<td>Mic input, line output</td>
</tr>
<tr>
<td>14/15</td>
<td>LINE2</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>16/17</td>
<td>MIC2</td>
<td>Int. Mic</td>
<td>Mic input</td>
</tr>
</tbody>
</table>

**POWER GENERATE**

*Layout*
20 mil
Connecting a 10 K external pull-down resistor makes the base address sample low, setting the Index-Data pair at 2Eh-2Fh.

VISHAY FIR/CIR Module
Place C581, C583 near Pin1 and Pin6

Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32

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Title
Size Document Number RevDate: Sheet

Wednesday, April 26, 2006
GOLDEN FINGER FOR DEBUG BOARD

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

TOP VIEW

A15 (B1)
A14 (B2)
A2 (B14)
A1 (B15)

(BOTTOM VIEW)
102V_S0 should not exceed 108V_S0 by more than 0.6V.
For TPS51120, Vout=5V

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 36m ohm.

Vout=1V*(R1+R2)/R2
For New Card/ MINI Card solution

1D5V
Iomax=1A

1D05V_S0
Iomax=3A

OD9V
Iomax=1A

1D8V_S5
Iomax=300mA

1D5V
Iomax=120mA

1D8V_S5
Iomax=120mA

Rh/RL=(Vout/0.8)-1

Vo=0.8*(1+(R1/R2))

Vo(cal.)=1.053V

20060217PM

OCP>6A

OCP>2A

Rh/RL=(Vout/0.8)-1

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Wednesday, April 26, 2006