### Change Notes List

**KARIA - DISCRETE**

#### 03/11/08:
- **Page 51**: Change R118 to 287K ohm from Vox information.
- **Page 43**: Change R582.2 to +3VALW from +3VS to power U89.39 (3V3)
- **Page 45**: Change R232 to NO INSTALL
- **Page 30**: Remove D48, connect signal directly to ADP_PRES, and uninstall R558
- **Page 27**: Reserve a 1u 0603 cap (NO INSTALL) on MC2_DISALBE (same as MC1_DISABLE)
- **Page 19**: Add a 0 ohm series on PLT_RST# at U113.4
- **Page 33**: Add a 0 ohm series on PM_PWROK, R at R175.2
- **Page 13**: Uninstall BGA_CRACK circuit: U115, U116, R740, R744, R801, & R802
- **Page 23**: Uninstall BGA_CRACK circuit: U117, U118, R803, R804, R805, & R806
- **Page 39**: Change R710 (SHDN_SEL) to 15K 1% to use Internal Diode for H/W critical shutdown
- **Page 57**: Add a discharging FET (gate connect to Q15.D) on 3.3V_DELAY at Q42.D
- **Page 25**: May require a discharging FET for +3VM_LAN at Q39.D
- **Page 32**: May need to change RGB q-switches power to +3VALW or +5VS (depending on wavy impact)
- **Page 51**: Change R97 to 33K from 1.27K
- **Page 41**: Change DAUGHT1 pin 52 and pin 54 to +5VS from +5VALW
- **Page 41**: Remove ICH_SMB_CLK/DATA from DAUGHT1 pin 32 and 34

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**Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Layout notes:
1. DINV# signals through a ground referenced to VCC. Set the trace length to 1/2 the trace length of the package. Make sure the trace length is shorter than 0.5".
2. For trace lengths greater than 0.5", use test points to ensure proper signal integrity.
3. Adjacent traces may need to be separated by 0.025" to prevent crosstalk.
4. Use a ground plane to minimize noise and improve signal quality.
5. Ensure the test points are accessible for testing and maintenance.
6. Use proper soldering and via techniques to ensure reliable connections.
7. Follow the manufacturer's guidelines for trace width and material specifications.
Please these inside socket cavity on L6 (North side Secondary)

layout note: "1DSV_VCCA_S0" as short as possible

Please these inside socket cavity on L6 (South side Secondary)

layout note: Place as close as possible to the CPU VCCA pin.

Please these inside socket cavity on L6 (North side Primary)

layout note: Place as close as possible to the CPU VCCA pin.

Please these outside socket cavity on L6 (North side Secondary)

layout note: Place as close as possible to the CPU VCCA pin.

Please these inside socket cavity on L6 (South side Primary)

layout note: Place as close as possible to the CPU VCCA pin.

Please these inside socket cavity on L6 (North side Secondary)

layout note: Place as close as possible to the CPU VCCA pin.

+VCCP

Please these inside socket cavity on L6 (North side Secondary)

layout note: Provide a test point with no diode to connect a differential probe between VCCSENSE and VDDSENSE at the location where the two 64-Bit pins reside to decode the 64-Bit data transmission line.
Modification A26 to reserved pin
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

Place these Caps near DM1

Place the Cap near MCH

Place these Caps near DM2

DDR2 Termination Resistor
CRT

CRT Termination/EMI Filter
Place Close VGA Chip

Place Close Dock

Place Close CRT connector

Layout Note: HSYNC & VSYNC SHOULD BE ROUTED TO DOCK CRT CONN., THEN TO SYSTEM CRT CONN.
Layout Note:
Keep this R173 on top side and route differentially
Note: MDO[3..0]-- signals should route to RJ45 first then to DOCK CONN.
62.10076.011 & 62.10089.001 is SPI Socket part number

Keep traces of SPI as short as possible and keep trace spacing close to tails to any other signal (basically follow spec).

Mini-PCIE Card LED control circuit
Docking CONN. 164 PIN

Connect to Daughter BD

Place MODEM1 near Docking connector

For TIP and Ring cut all layers
The shield GND is needed for SD_CLK(ND1009). Also, the wider-width (more than 0.02inch) trace for ND1009 should be used.

Wistron Corporation
217, Sec. 1, Han Tai Rd., Hsinchu, Taoyuan, Taiwan, R.O.C.
CPU TEMP:

H_THERMDA and H_THERMEC routing 10mil trace width and spacing. Locate Capacitor near thermal diode.

GPU TEMP:

GPU DIE TEMP:

REMOTE2+ and REMOTE2- routing 10mil trace width and 10 mil spacing.
TI TPS51116 for 1D8V and 0D9V

<table>
<thead>
<tr>
<th>State</th>
<th>S3</th>
<th>S5</th>
<th>VDDR</th>
<th>VTTREF</th>
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<tbody>
<tr>
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<td>H1</td>
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<td>On</td>
<td>On</td>
<td>On</td>
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<tr>
<td>S3</td>
<td>Lo</td>
<td>H1</td>
<td>On</td>
<td>On</td>
<td>Off (H-L)</td>
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<tr>
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<td>Lo</td>
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84.07636.037 SI7636DP
Id=28A Qip=32-50nC
Rdsom=4.8mΩ

CYNTEC 0.82mH
Iid=13A, 6.5±6.9mA
DCR=6.7mΩ

Kemet 330μF
2.5V ESR=9mΩ,
Triipple=3.7A

0D9V
Iomax=1A