Compal confidential

Schematics Document

Mobile Yonah uFCPGA with Intel Calistoga_GM/PM+ICH7-M core logic

2006-05-19
REV: 0.1
### Voltage Rails

<table>
<thead>
<tr>
<th>State</th>
<th>+B</th>
<th>+5V</th>
<th>+5VALM</th>
<th>+1.8V</th>
<th>+5VS</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
</tr>
<tr>
<td>S1</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td>O</td>
</tr>
<tr>
<td>S3</td>
<td>O</td>
<td>O</td>
<td>O</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>S5 S4/AC</td>
<td>O</td>
<td>O</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>S5 S4/ Battery only</td>
<td>O</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>S5 S4/AC &amp; Battery don't exist</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

O MEANS ON
X MEANS OFF

### PCI Devices

<table>
<thead>
<tr>
<th>External</th>
<th>IDSEL#</th>
<th>REQ/GNT#</th>
<th>PIRQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>CARD BUS &amp; 1394</td>
<td>AD22</td>
<td>2</td>
<td>C,D,E,G</td>
</tr>
<tr>
<td>RealTek B100CL</td>
<td>AD24</td>
<td>1</td>
<td>E</td>
</tr>
</tbody>
</table>

**Load BOM check item**
1. U31 GM/PM/GML part number
2. U6 ICH7 part number

**BOM:** 43144132L01 (GM) 43144132L02 (GML)

**Jump-Short:**
- PJP4, PJP6, PJP7, PJP8, PJP10, PJP12, PJP14, PJP18, PJP19, PJP20, PJP25
+1.5v is a power source required by the PL clock generator on the processor silicon.

VCCP is the FSB rail of the processor and GMCH.

Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal.

Length match within 25 mils.
The trace width 18 mils space 7 mils.
Mid Frequency Decoupling

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**CPU Bypass capacitors**

- CAPACITOR <6/19> Remove C578 820uF
- CAPACITOR <6/19> Remove C37 330uF
- CAPACITOR Place these inside socket cavity on L8 (North side, Secondary Layer)
- CAPACITOR Place these capacitors on L8 (North side, Secondary Layer)
- CAPACITOR Place these capacitors on L8 (South side, Secondary Layer)
- CAPACITOR Place these capacitors on L8 (North side, Secondary Layer)

**ESR <= 1.5m ohm**
**Capacitor > 1980uF**
Strap Pin Table

CFG(2:0) have internal pull up
CFG(9:18) have internal pull down

<table>
<thead>
<tr>
<th>CFG0</th>
<th>001 = 667MHz x FSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>CFG1</td>
<td>0 = DMI x 2</td>
</tr>
<tr>
<td>CFG2</td>
<td>0 = DMI x 4</td>
</tr>
<tr>
<td>CFG3</td>
<td>0 = Dynamic ODT Enabled</td>
</tr>
<tr>
<td>CFG4</td>
<td>1 = Dynamic ODT Disabled</td>
</tr>
<tr>
<td>CFG5</td>
<td>1 = Normal Operation (Default)</td>
</tr>
<tr>
<td>CFG6</td>
<td>0 = Lane Reversal Enable</td>
</tr>
<tr>
<td>CFG7</td>
<td>0 = Reserved</td>
</tr>
<tr>
<td>CFG8</td>
<td>0 = Normal Operation</td>
</tr>
<tr>
<td>CFG9</td>
<td>0 = Mobile Yonah CPU</td>
</tr>
<tr>
<td>CFG10</td>
<td>0 = No SDVO Device Present</td>
</tr>
<tr>
<td>CFG11</td>
<td>1 = SDVO Device Present</td>
</tr>
<tr>
<td>CFG12</td>
<td>0 = Only PCIE or SDVO is operational</td>
</tr>
<tr>
<td>CFG13</td>
<td>1 = PCIE/SDVO are operating simultaneously</td>
</tr>
<tr>
<td>CFG14</td>
<td>0 = Reserved</td>
</tr>
<tr>
<td>CFG15</td>
<td>0 = 1.5V</td>
</tr>
<tr>
<td>CFG16</td>
<td>0 = Dynamic ODT Enabled</td>
</tr>
<tr>
<td>CFG17</td>
<td>0 = Normal Operation</td>
</tr>
<tr>
<td>CFG18</td>
<td>0 = Mobile Yonah CPU</td>
</tr>
<tr>
<td>CFG19</td>
<td>0 = Lane ODT Enabled</td>
</tr>
<tr>
<td>CFG20</td>
<td>0 = Reserved</td>
</tr>
<tr>
<td>CFG21</td>
<td>0 = Normal Operation</td>
</tr>
<tr>
<td>CFG22</td>
<td>0 = Mobile Yonah CPU</td>
</tr>
<tr>
<td>CFG23</td>
<td>0 = SDVO Device Present</td>
</tr>
<tr>
<td>CFG24</td>
<td>1 = SDVO Device Present</td>
</tr>
<tr>
<td>CFG25</td>
<td>0 = Only PCIE or SDVO is operational</td>
</tr>
<tr>
<td>CFG26</td>
<td>1 = PCIE/SDVO are operating simultaneously</td>
</tr>
</tbody>
</table>

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Callistoga (5/6)
Layout Note:
Place near JP42

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V supplies

Layout Note:
Place these resistors closely JP42, all trace length Max=1.5"
FOR POWER BUTTON BACKLIGHT SYSTEM POWER

For PR

INDICATE LED
BID definition,
High (3.3V): Before SI2 type D KB(17")
Low (0V): Before SI2 type C KB(15")

2.2V(R325=1K,R333=2K): After PV type D KB(17")
1.65V(R605=2K,R333=2K): After PV type C KB(15")

3/29 Design Change

To eliminate coupling noise

Security Classification

Compal Electronics, Inc.

Issue Date 2005/03/15

Deciphered Date 2005/03/15

TID

EC KB910L(LPC)

Revision 1.0

Lot 3

Revised by

Compal Electronics, Inc.
Charger

65W, Iadp=0~3.0A

65W(1.40V(-1 level); 1.30V (+1 level)

65W=>1.202V

5.0V

4.2V

CC=0.4~2.8A

3S2P/3S4P : 13.5V--> BATT_OVP = 2.0V
(BAT_OVP=0.14753 *BATT+)

<31> BATT_OVP

<31> AIR_ACN

<31>  BATT++

<31> BAT_TCS

<31> DTC115EA_SC70

<31> DTC115EUA_SC70

<31> PQ4

Security Classification

Compal Secret Data

Issued Date

2006/04/03

Deciphered Date

2007/04/03

TID

Charger

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Battery Connect/OTP

PH1 under CPU bottom side:
- CPU thermal protection at 90 +/– 3 degree C
- Recovery at 50 +/– 3 degree C

SMART
- Battery:
  1. BATT+
  2. SMBD
  3. SMC
  4. Res
  5. Temp
  6. GND

PJPB1 battery connector

Security Classification
Compal Secret Data

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