

Cover Sheet	1
Block Diagram	2
Intel LGA775 CPU - Signals	3
Intel LGA775 CPU - Power & GND	4-5
Intel Grantsdale - CPU & Memory Signals	6-7
Intel Grantsdale - PCI Express Signals & GND	8-9
Intel ICH6 - PCI & DMI & CPU & IRQ	10
Intel ICH6 - LPC & ATA & USB & GPIO & POWER	11-12
Clock -CY28416 & FWH	13
LPC I/O - W83627THF	14
Azalia CMI 9880	15
LAN -- Marvell 88E8053	16
DDR2 System Memory 1 & 2	17
DDR 2 Termination Resistors & 2.5V DAC	18
PCI EXPRESS X16 Slot	19
PCI Slot 1 , 2 & 3	20
USB Connectors	21
ATX , VGA Connetcors & Front Panel	22
MS-7 ACPI Controller & MS-6 Plus	23
VRM 10.1 - Intersil 6565ACV + HIP 6602B +HIP 6601B	24
FAN & ICH6 IDE Connectors	25
VIA-6307 IEEE1394 Controller	26

# MS-7066

**Version 0B**  
**05/05/2004**

**CPU:**

**Intel Tejas & Prescott LGA775 Processor**

**System Chipset:**

**Intel 915 - GMCH (North Bridge)**

**Intel ICH6 (South Bridge)**

**On Board Chipset:**

**CLOCK -- CY28416**

**LAN -- Marvell 88E8053**

**LPC Super I/O -- W83627THF**

**Azalia CMI 9880**

**VIA-6307 IEEE1394 Controller**

**BIOS -- FWH EEPROM**

**Main Memory:**

**DDR 2 \* 2 (Max 2GB)**

**Expansion Slots:**

**PCI EXPRESS X16 SLOT**


**PCI2.3 SLOT \* 3**

**Intersil PWM:**

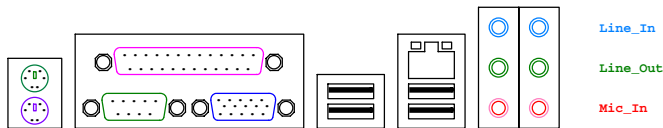
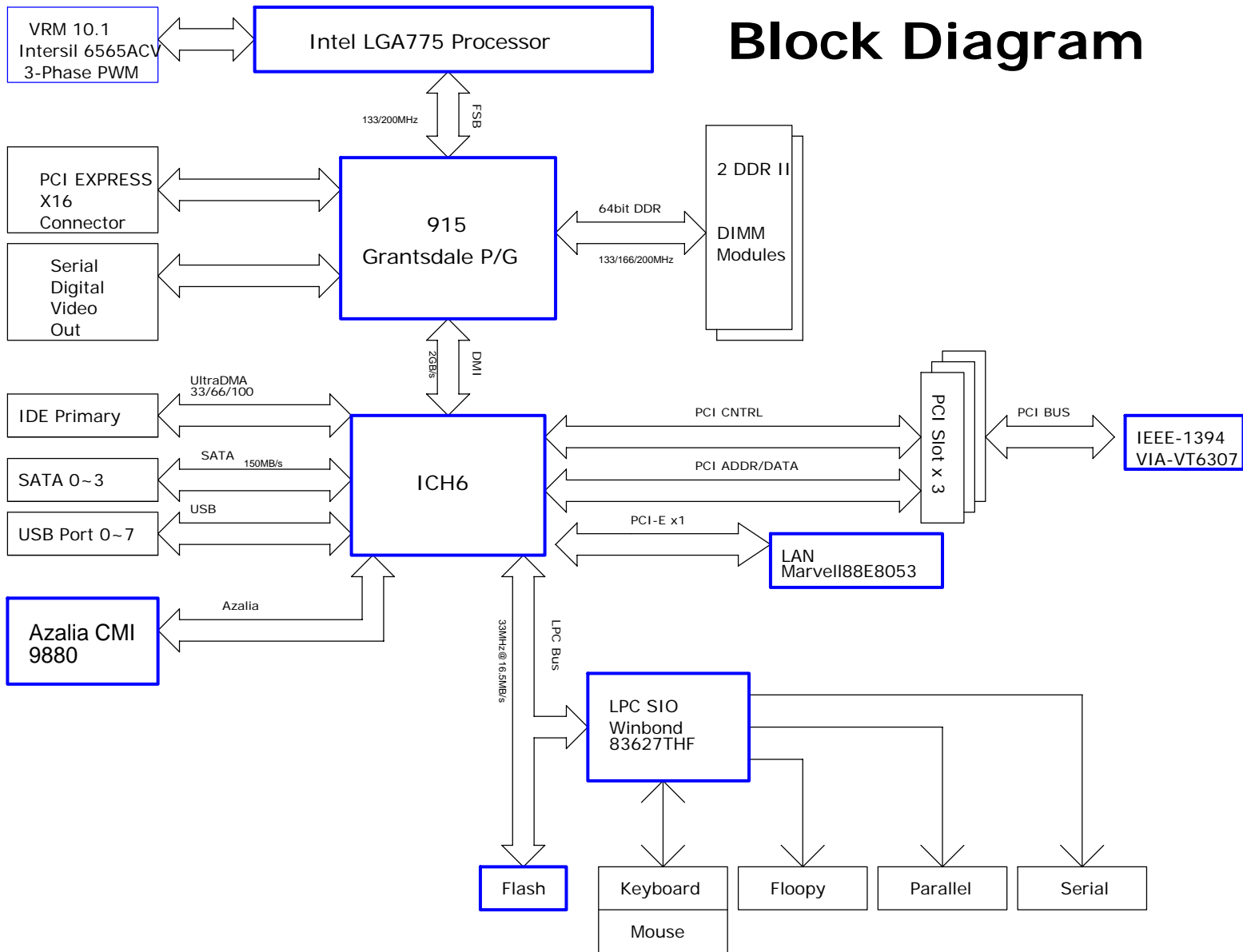
**Controller: HIP6565ACV3 Phase**

**Driver: HIP6602B \* 1**

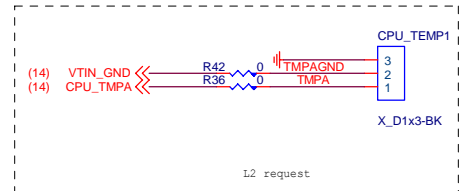
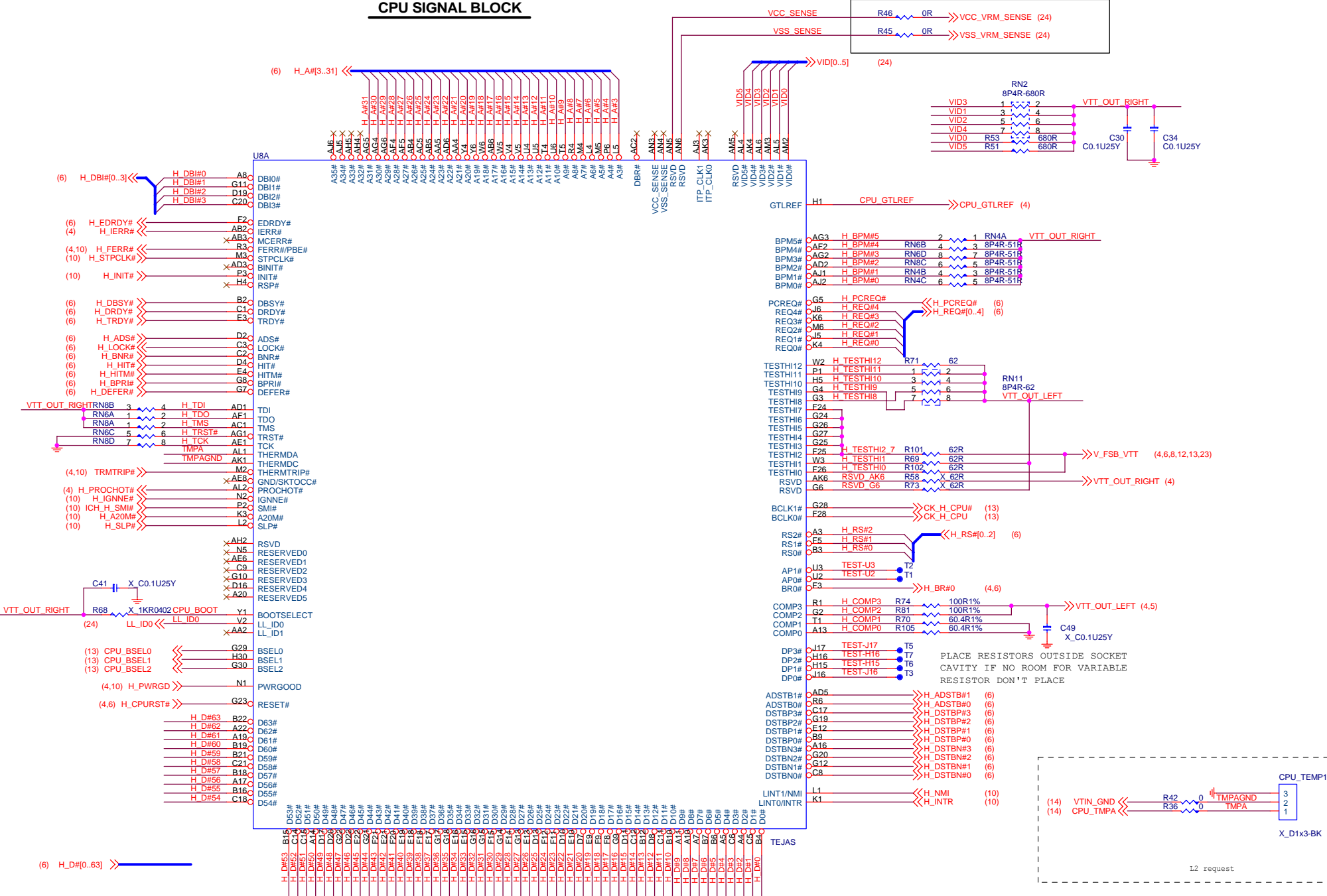
**HIP6601B \* 1**

		<b>MICRO-STAR INT'L CO., LTD.</b>	
Title COVER SHEET			
Size	Document Number	Rev	
	MS-7066	0B	
Date:	Friday, July 02, 2004	Sheet	1 of 30

# Block Diagram



# CPU SIGNAL BLOCK

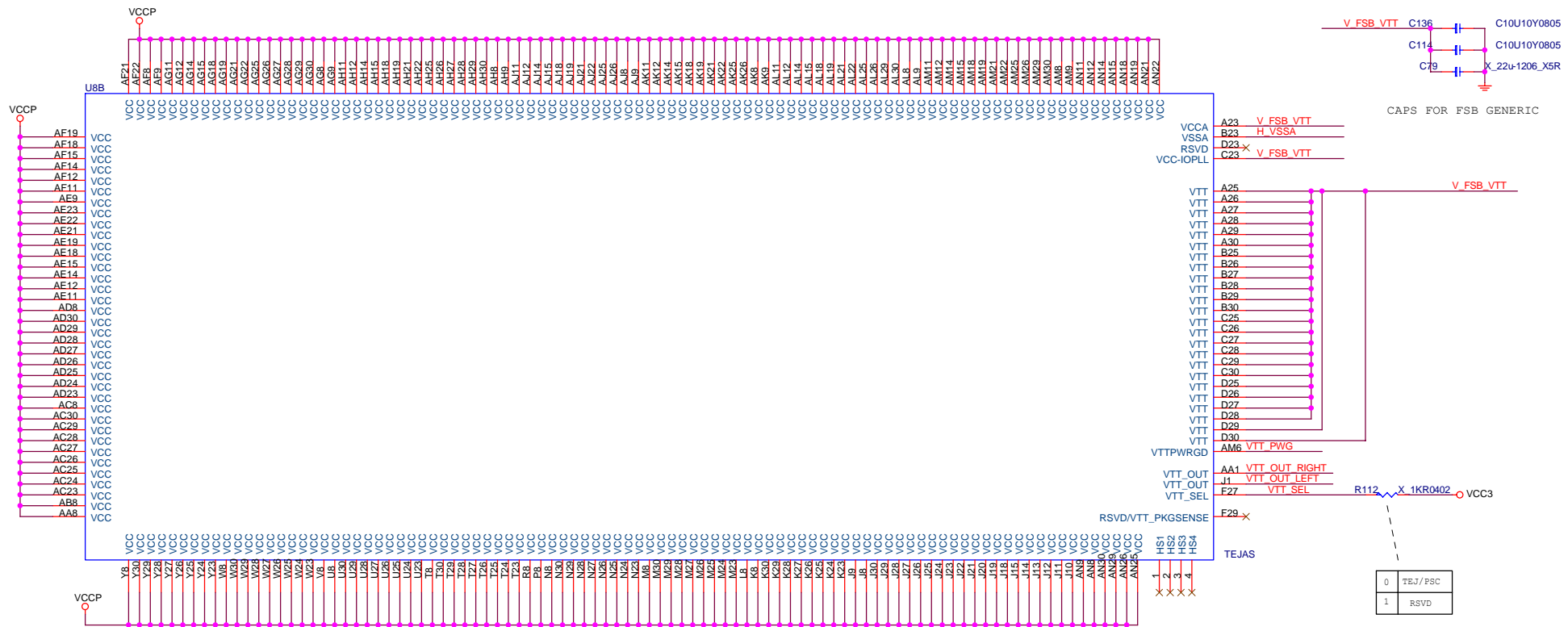


**MICRO-STAR IN'L CO., LTD.**

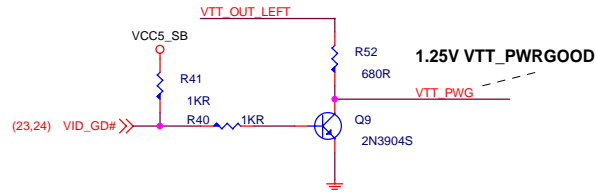
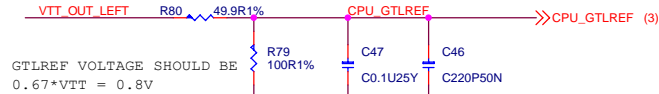
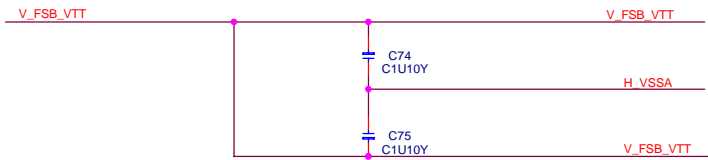
Title: Intel LGA775 CPU - Signals

Size: Document Number MS-7066 Rev: 0B

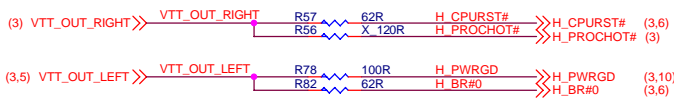
Date: Friday, July 02, 2004 Sheet 3 of 30



PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET  
TRACE WIDTH TO CAPS MUST BE SMALLER THAN 12MILS



PLACE AT CPU END OF ROUTE



PLACE AT ICH END OF ROUTE



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Title

Intel LGA775 CPU - Power

Size

Document Number

**MS-7066**

Rev

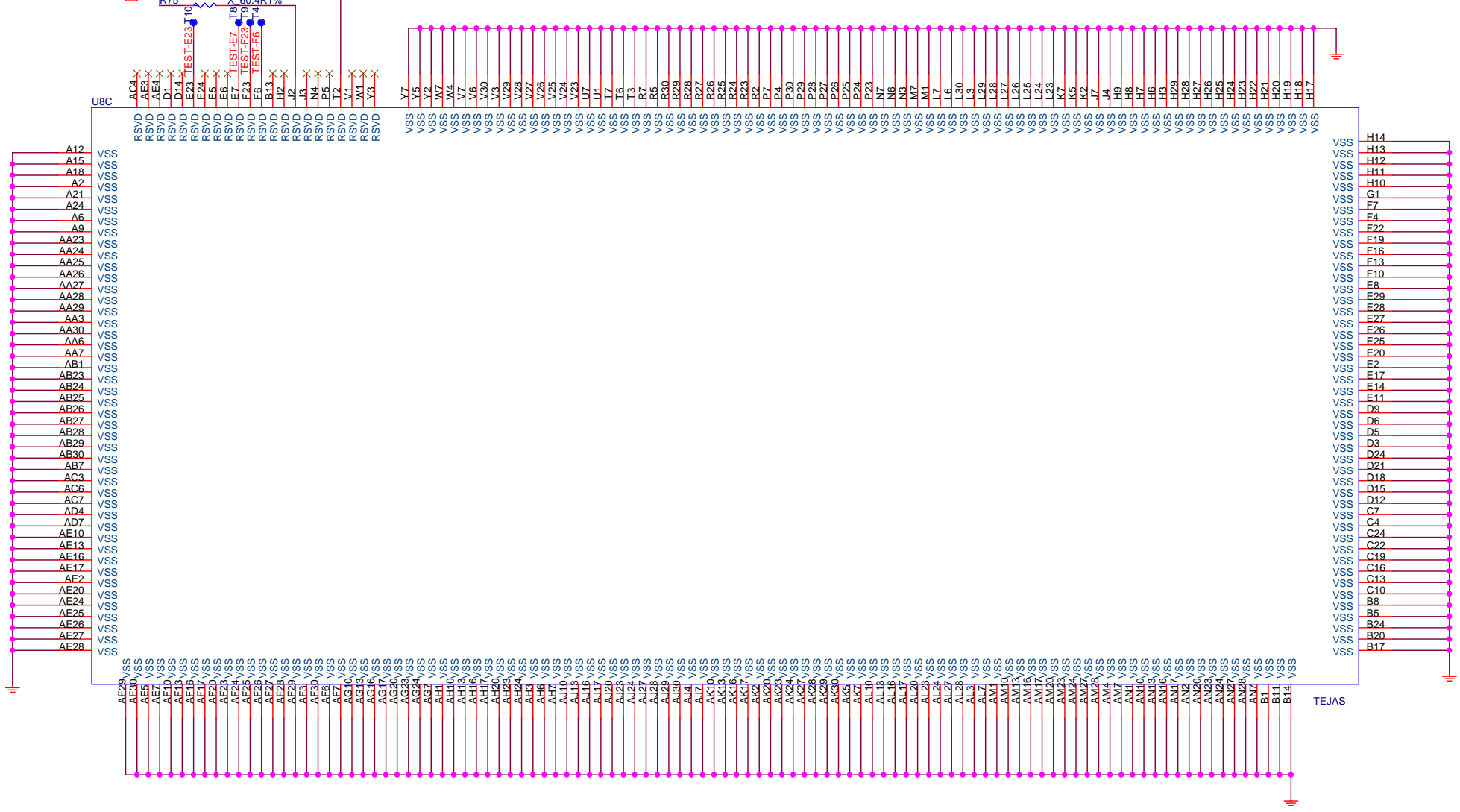
0B

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Date: Friday, July 02, 2004      Sheet 4 of 30

(3,4) VTT\_OUT\_LEFT

R72 X 60.4R1%  
R75 X 60.4R1%

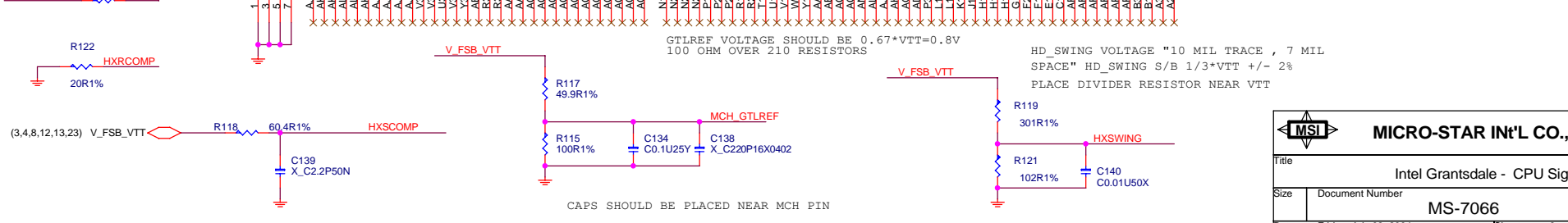
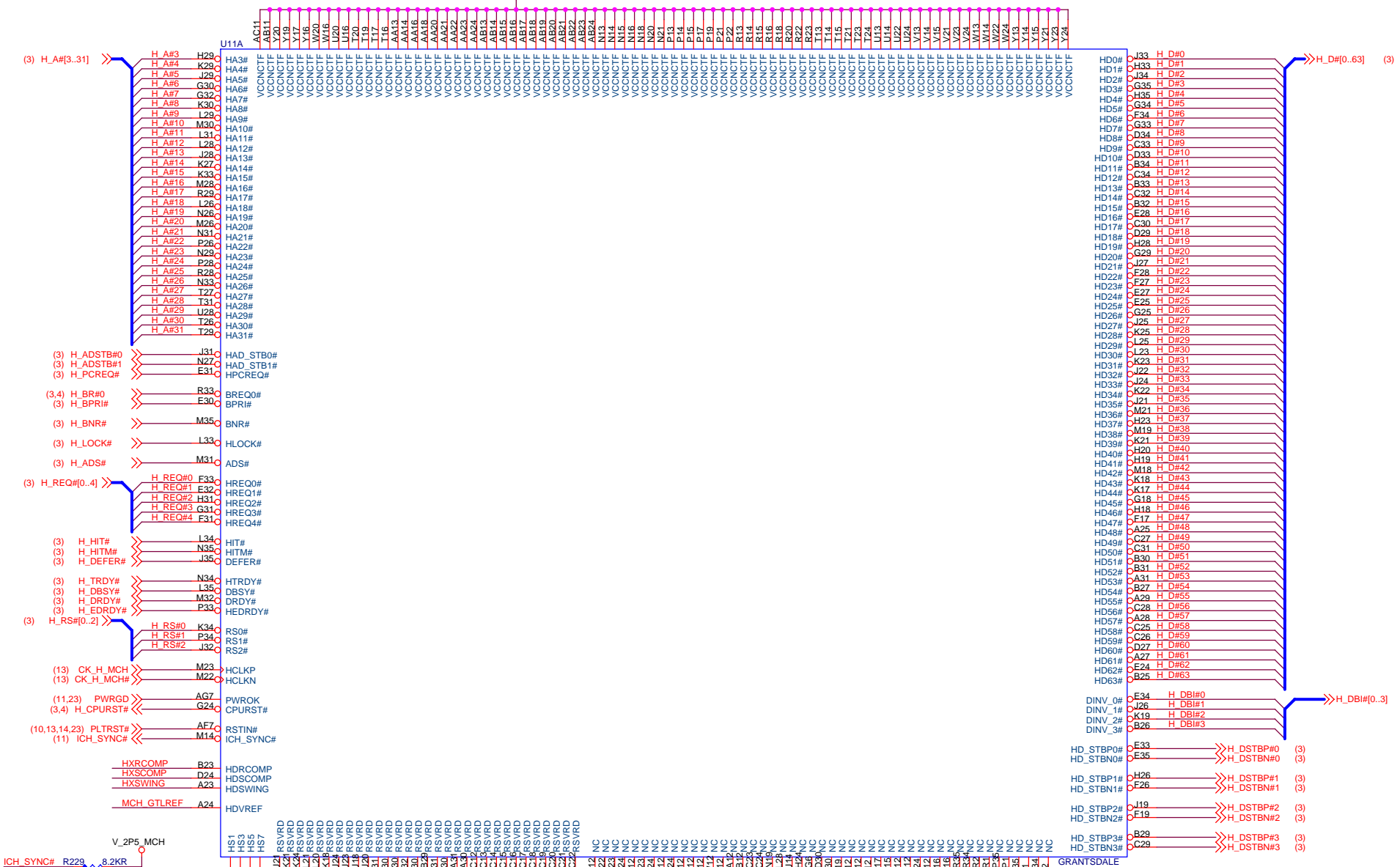


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Title		Intel LGA775 CPU - GND
Size	Document Number	MS-7066
Date:	Friday, July 02, 2004	Sheet 5 of 30

Rev  
0B

V\_1P5\_CORE

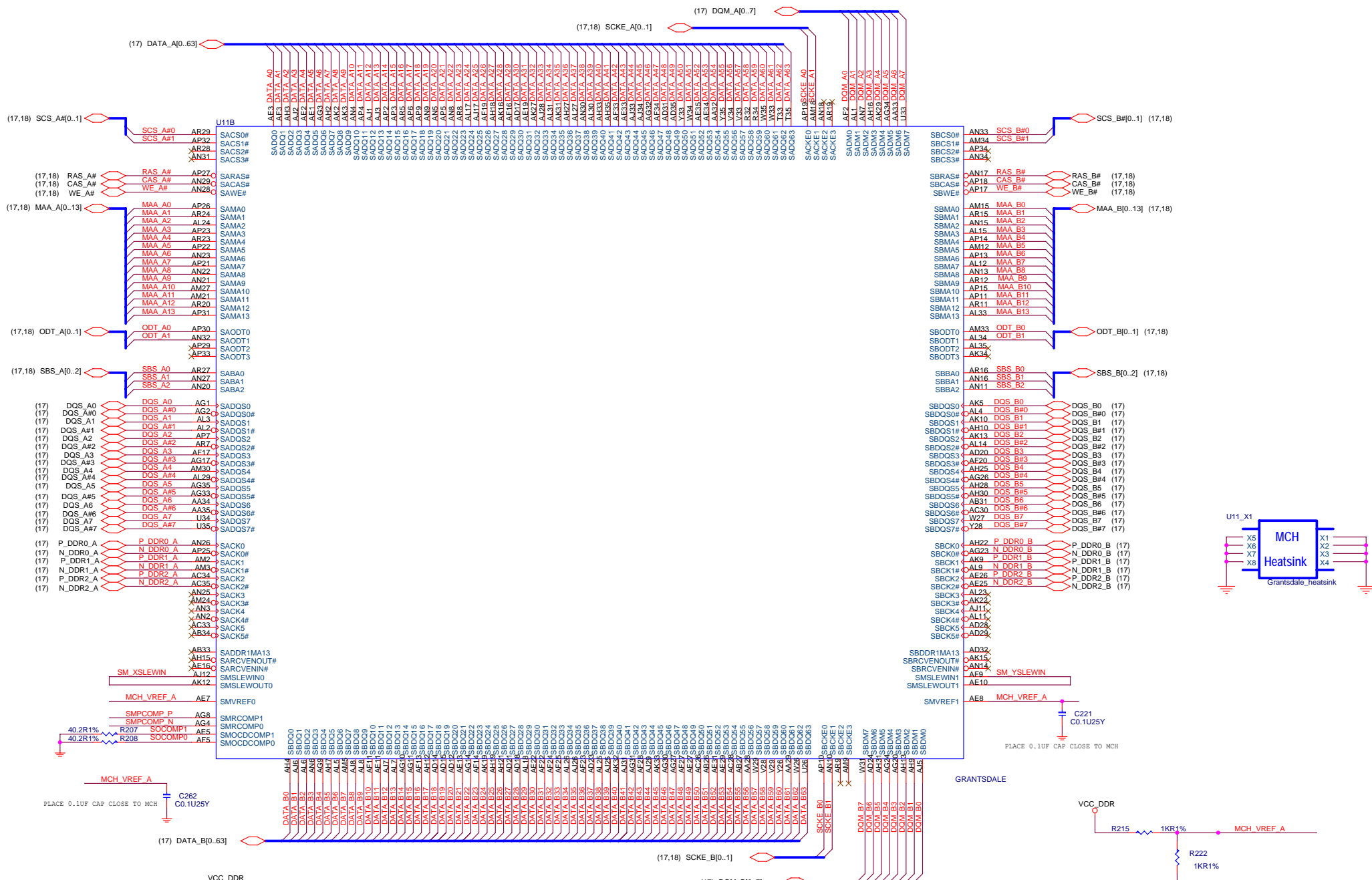


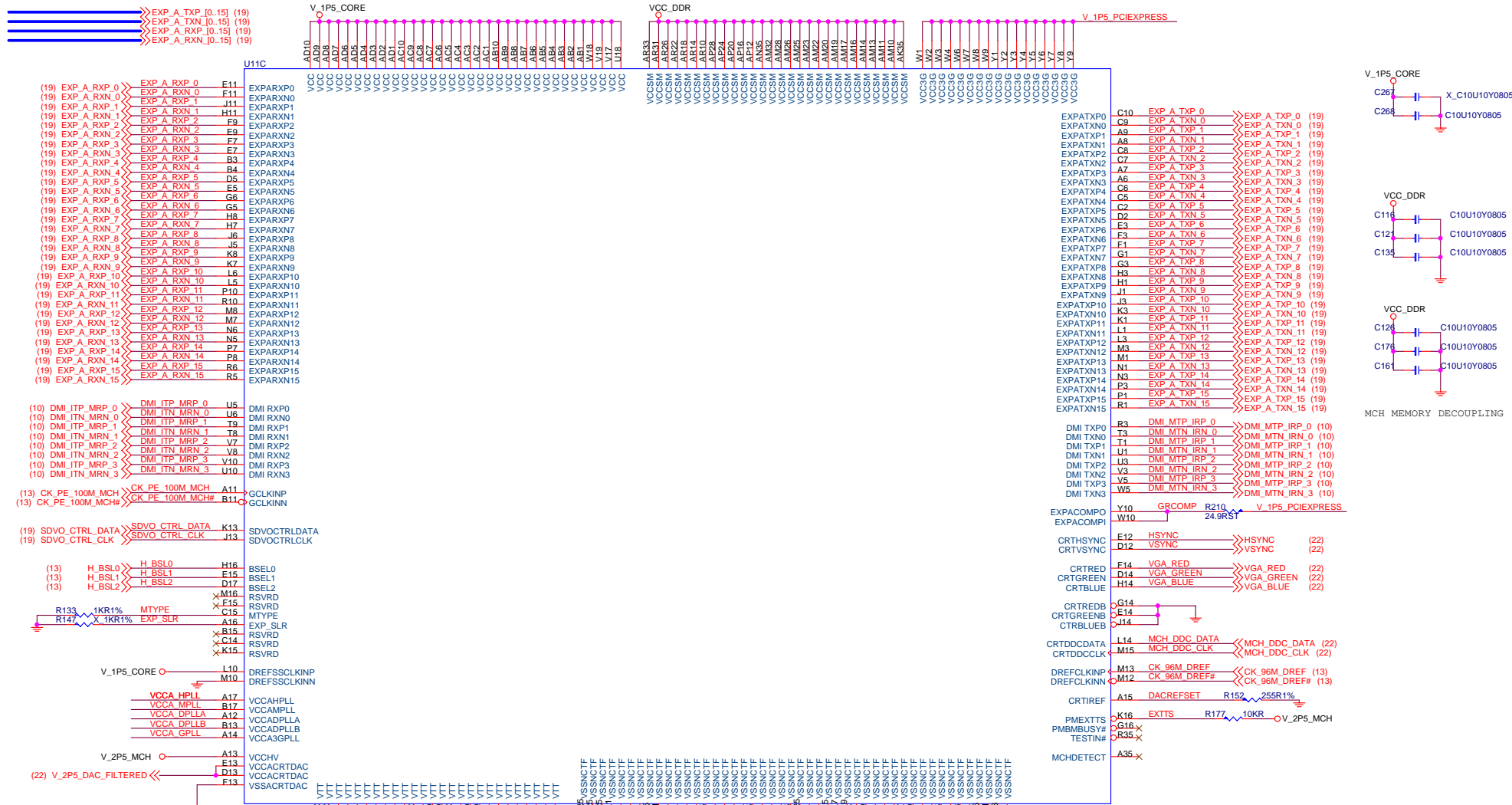
GTLREF VOLTAGE SHOULD BE  $0.67 * V_{TT} = 0.8V$   
 100 OHM OVER 210 RESISTORS

HD\_SWING VOLTAGE "10 MIL TRACE , 7 MIL SPACE" HD\_SWING S/B  $1/3 * V_{TT} \pm 2\%$   
 PLACE DIVIDER RESISTOR NEAR VTT

CAPS SHOULD BE PLACED NEAR MCH PIN

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Title Intel Grantsdale - CPU Signals		
Size	Document Number <b>MS-7066</b>	Rev 0B
Date: Friday, July 02, 2004	Sheet 6	of 30





BSEL	TABLE		PSB FREQUENCY
2	1	0	
0	0	1	1.33 MHz (533)
0	1	0	200 MHz (800)

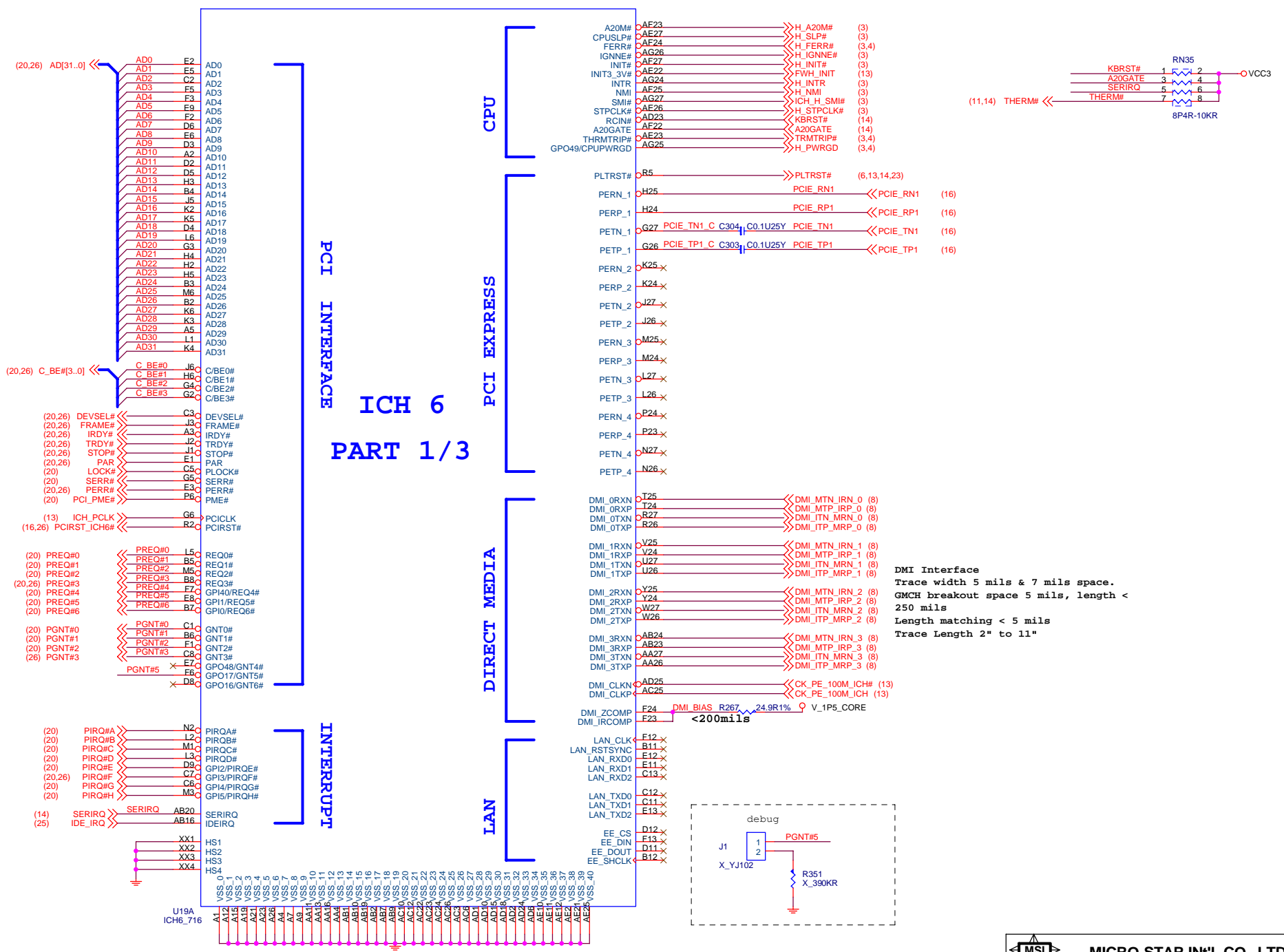
**MSI** MICRO-STAR INT'L CO., LTD.

Title: Intel Grantsdale PCI-Express & RGB Signals

Size	Document Number	Rev
	MS-7066	0B
Date:	Friday, July 02, 2004	Sheet 8 of 30



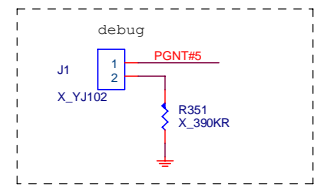




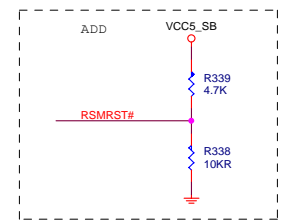
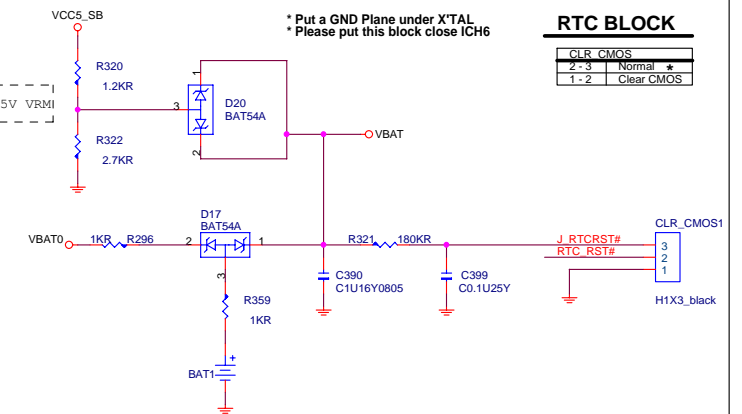
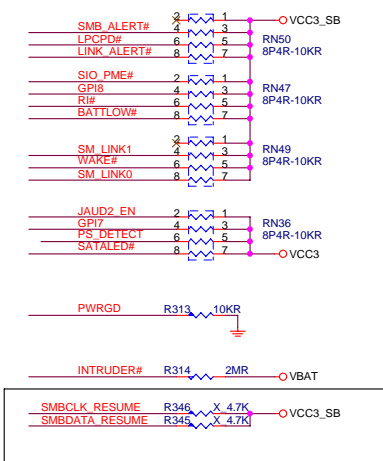
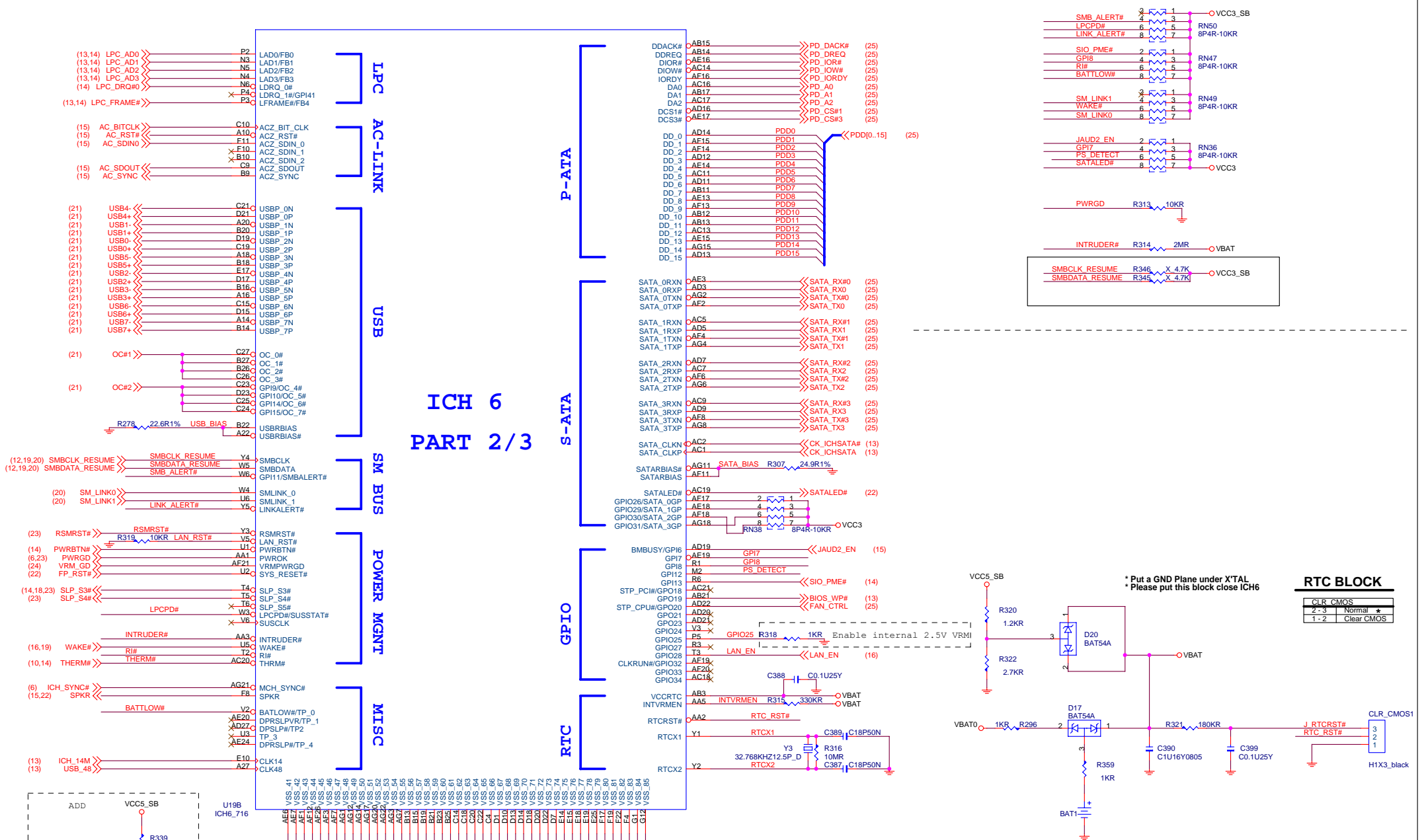
**ICH 6  
PART 1/3**



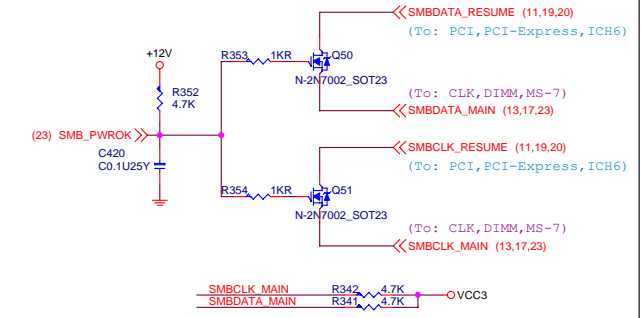
**DMI Interface**  
Trace width 5 mils & 7 mils space.  
GMCC breakout space 5 mils, length < 250 mils  
Length matching < 5 mils  
Trace Length 2" to 11"



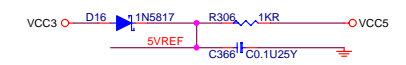
# ICH 6 PART 2/3



**SM BUS ISOLATION**



**5VREF Sequencing Circuit**



**ICH 6  
PART 3/3**

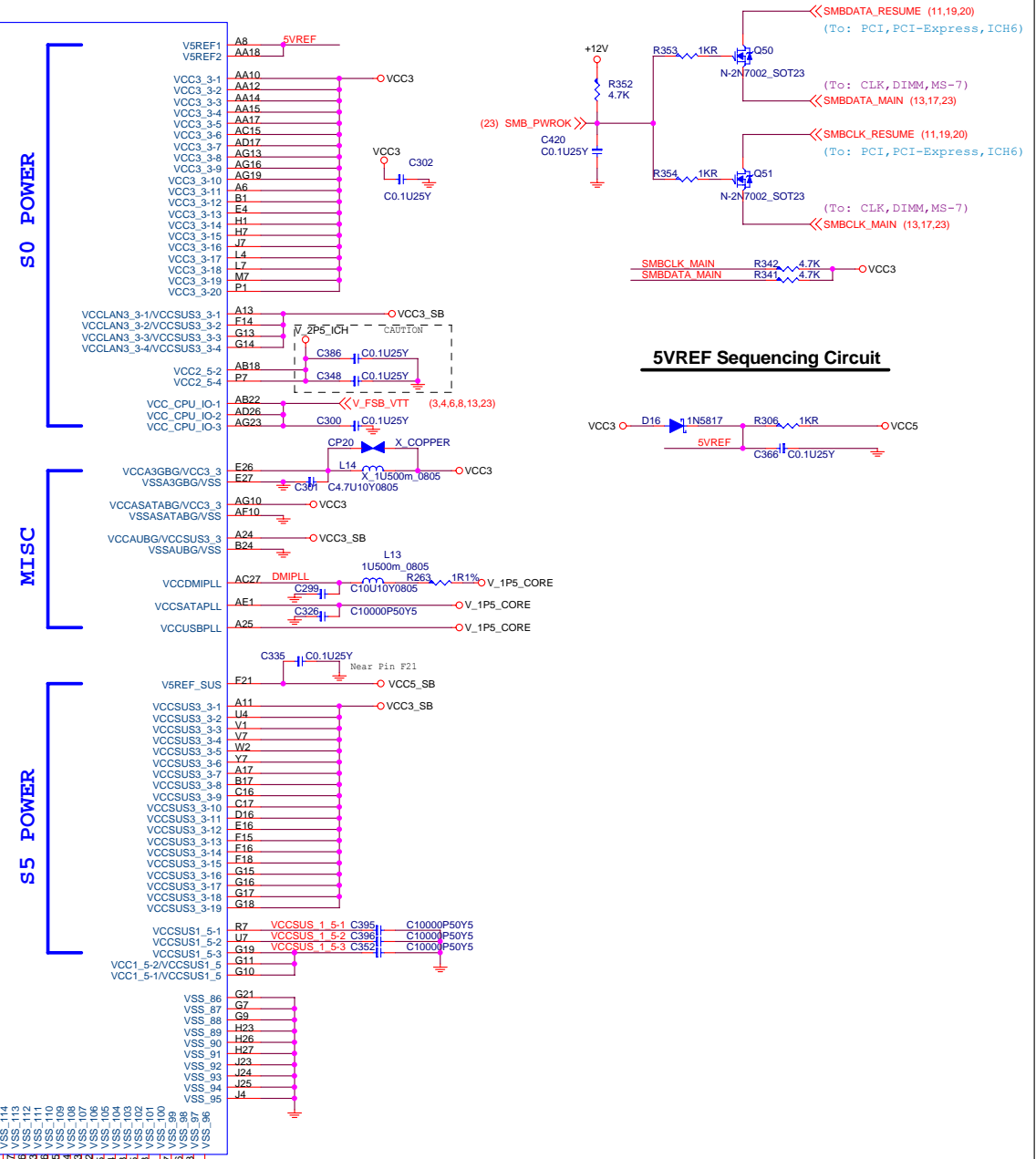
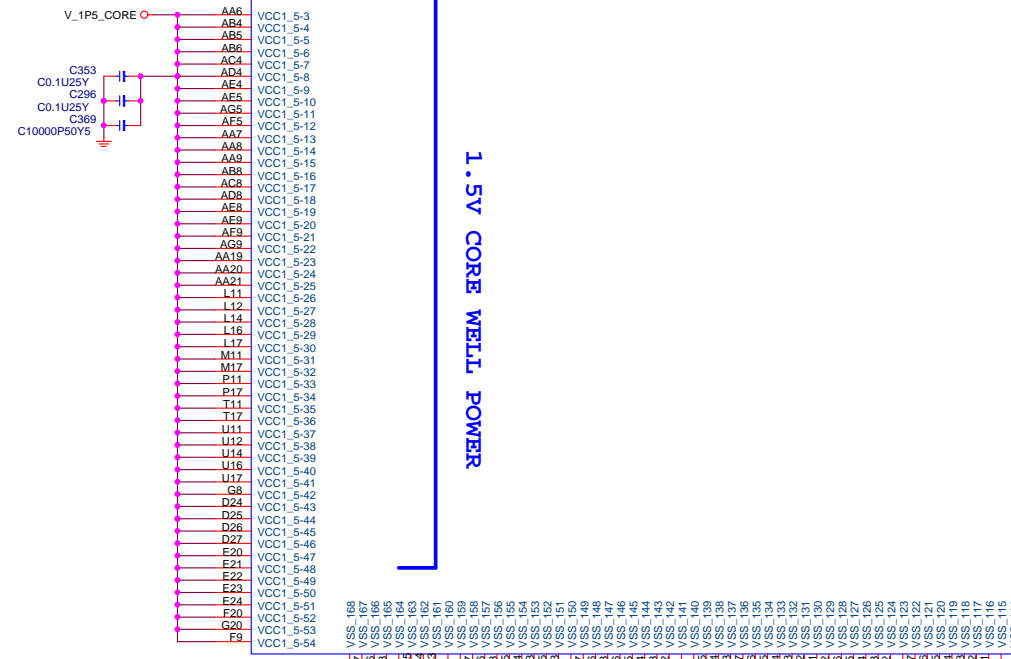
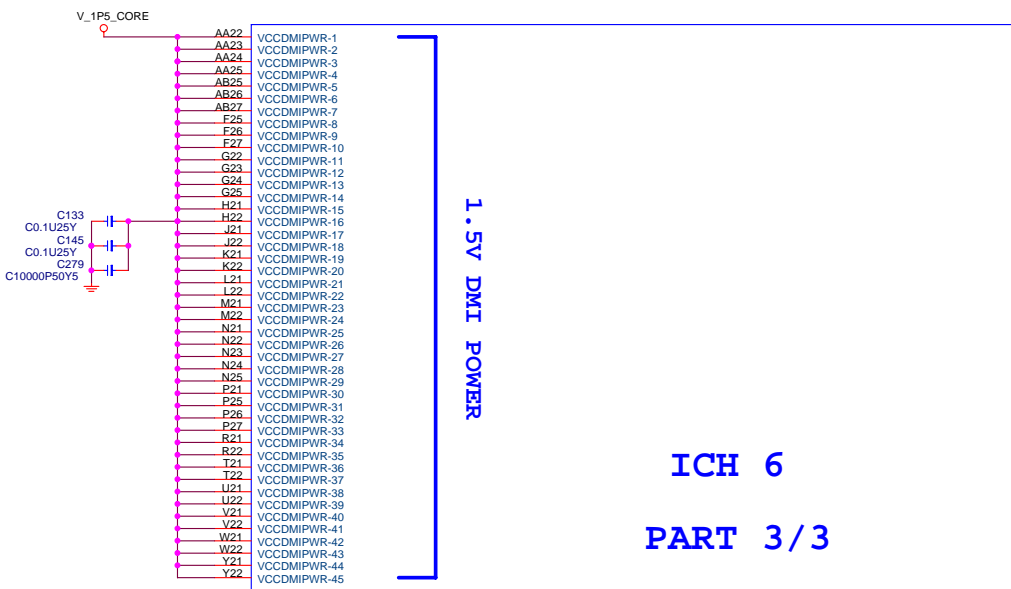
**1.5V DMI POWER**

**1.5V CORE WELL POWER**

**S0 POWER**

**MISC**

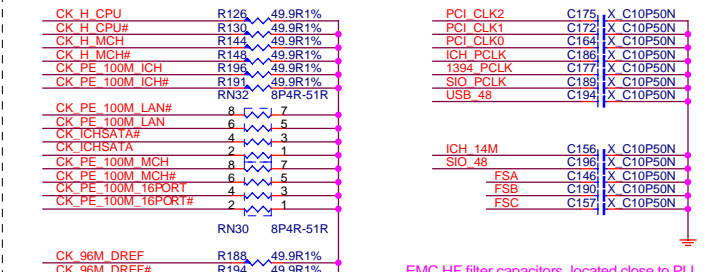
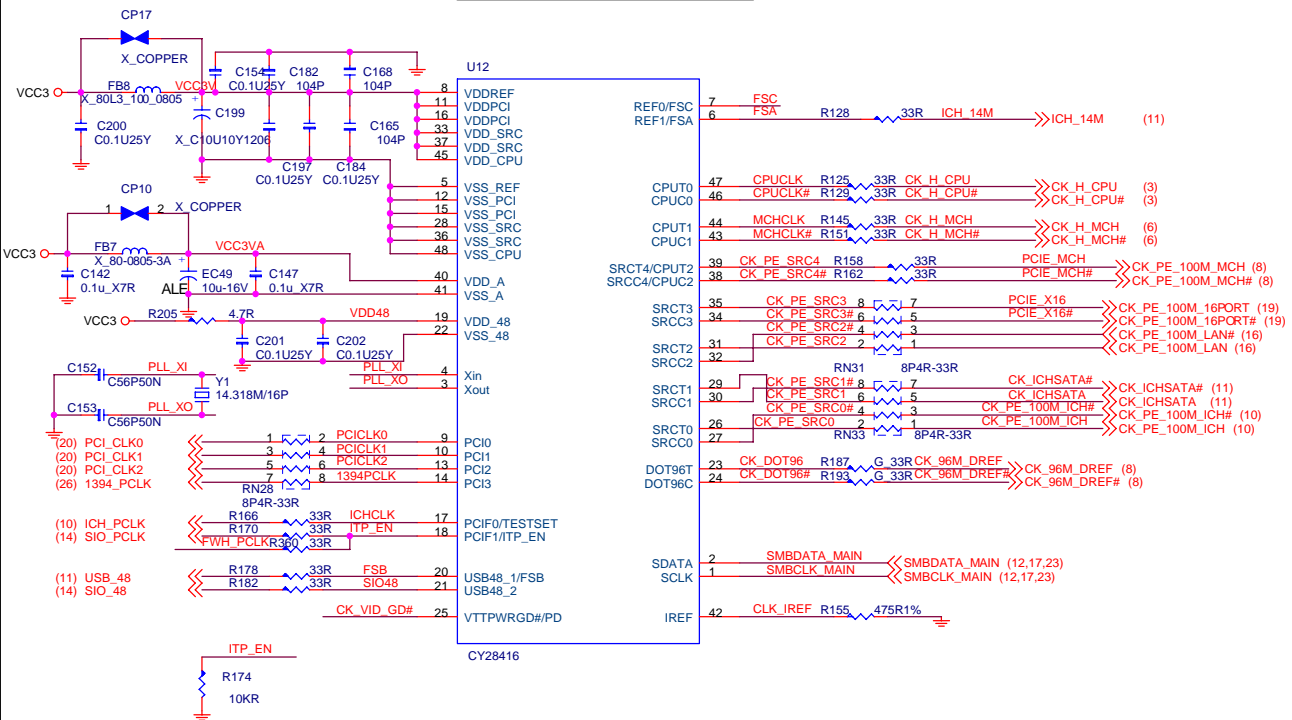
**S5 POWER**



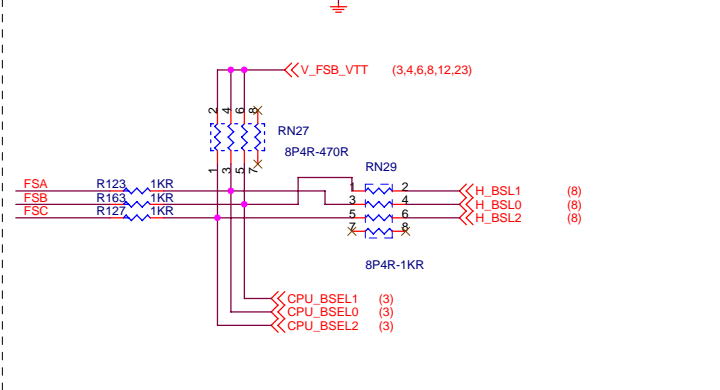
I19C  
ICH6\_716

### Clock Generator - CY28416

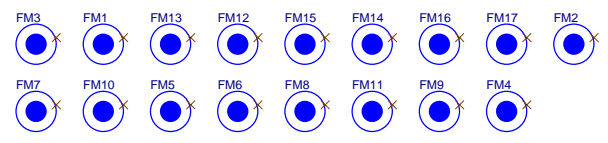
Trace length less than 0.5inches



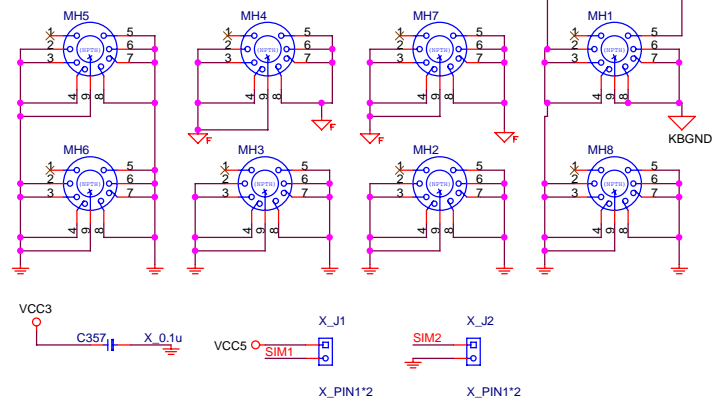
EMC HF filter capacitors, located close to PLL



### Optical Fiducial Marks



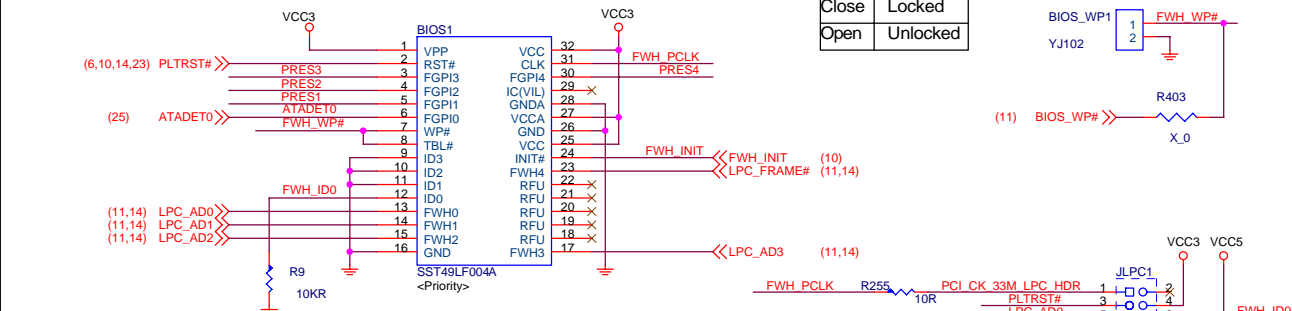
### Mounting Holes



### Firewire Hub (FWH)

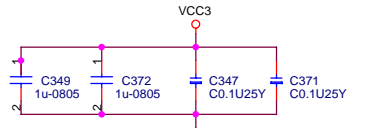
FWH_WP	
Close	Locked
Open	Unlocked

### FWH write protect



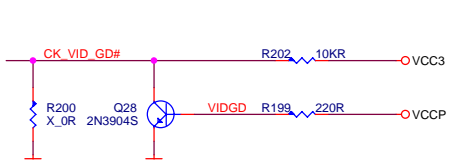
If you place the jumper very close to FWH bios socket, please use the same clock with FWH. But if you can not place it so close, please use another clock to support it.

### FWH DECOUPLING CAPACITORS

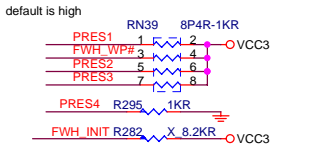


Place Cap. as Close to FWH< 350 mil

### Clock Generator VTT Power Down Block



### FWH Resistors

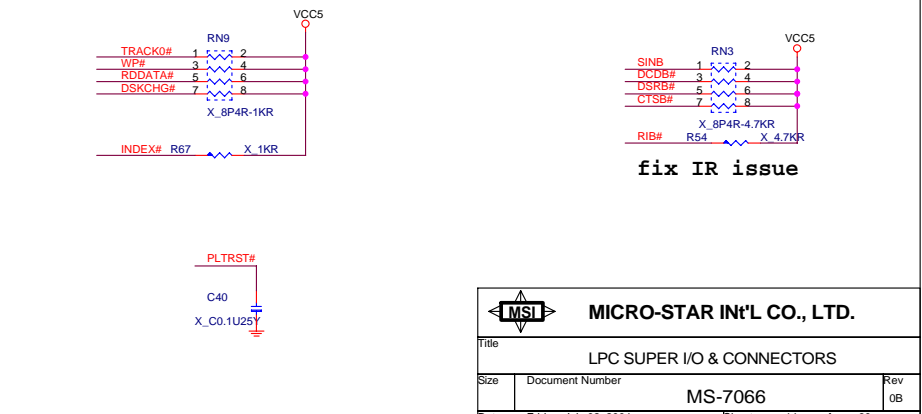
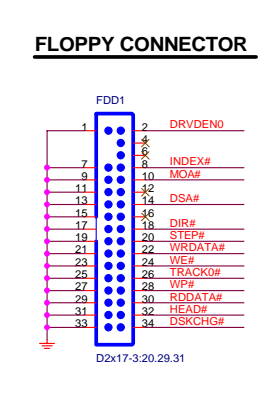
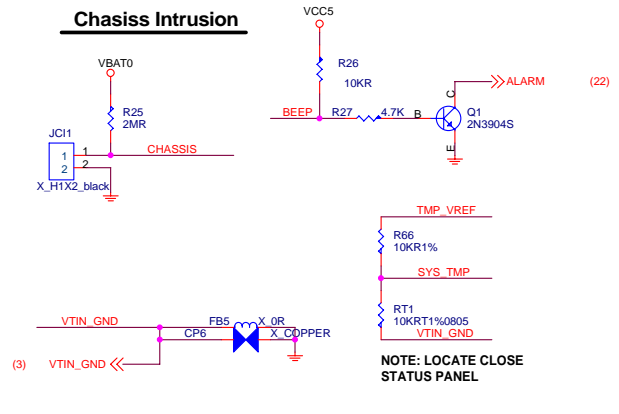
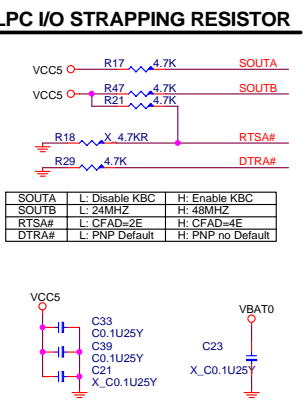
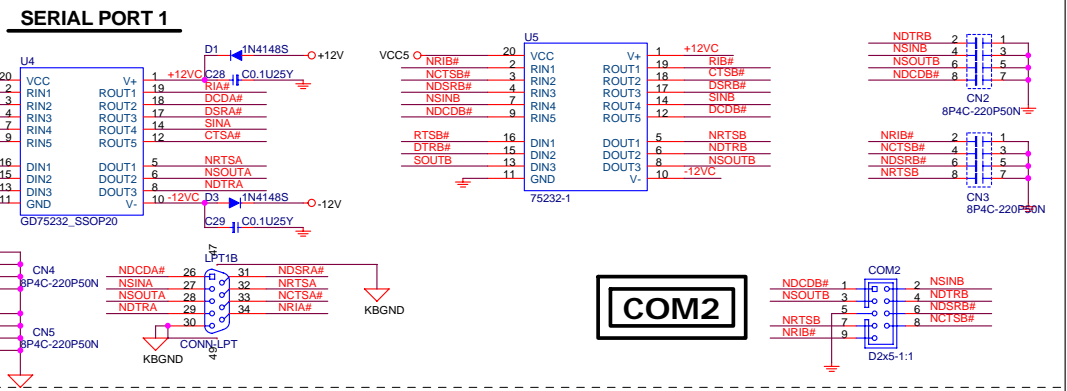
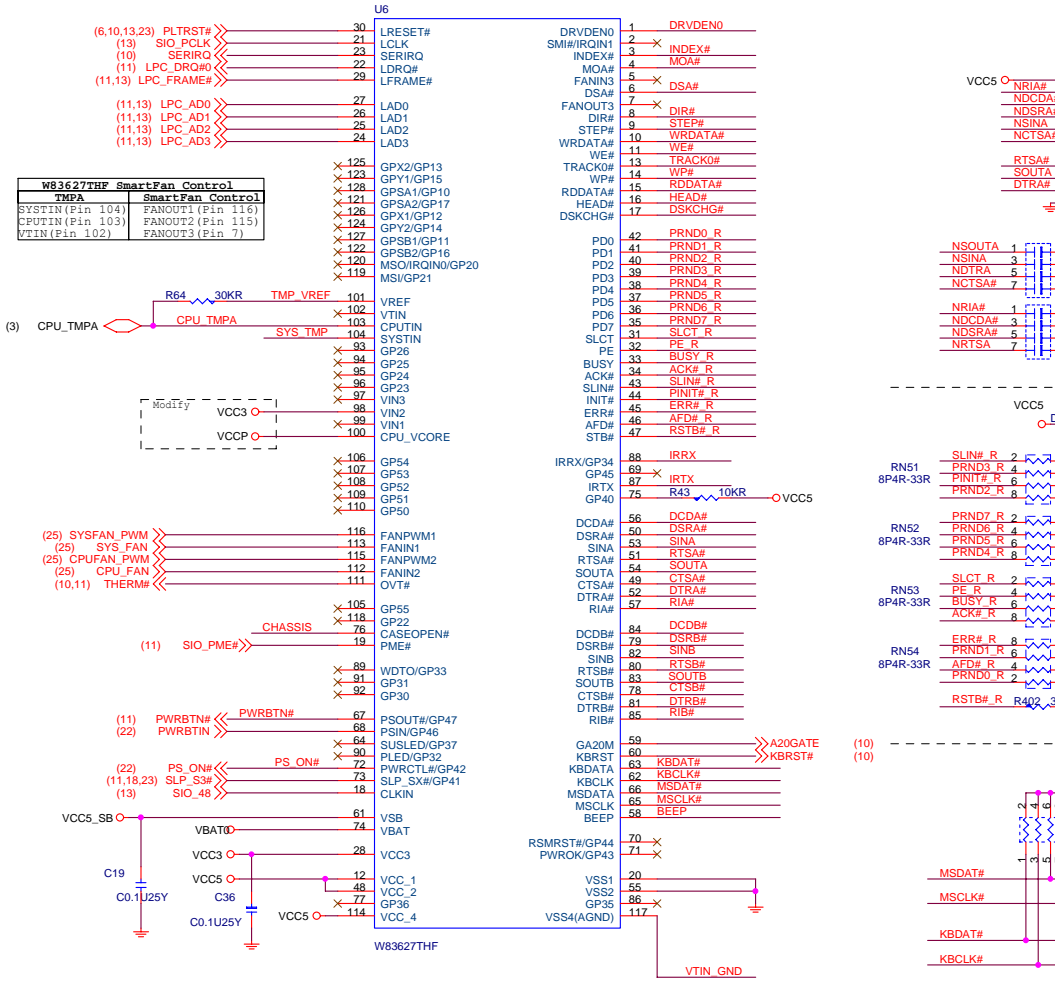


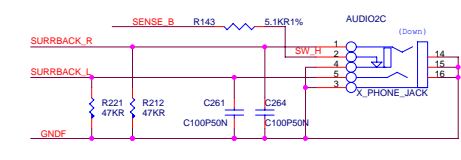
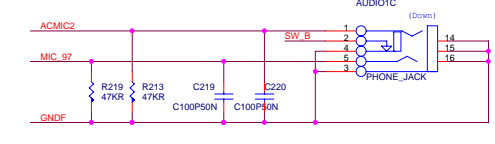
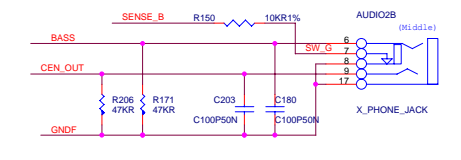
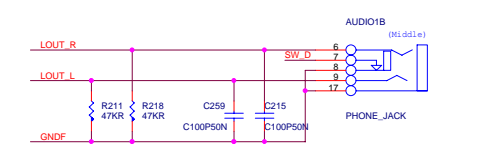
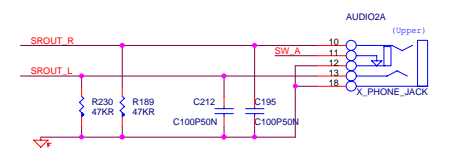
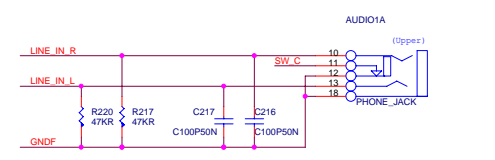
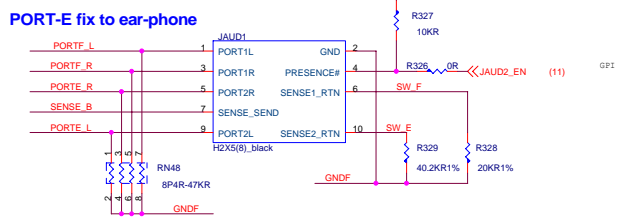
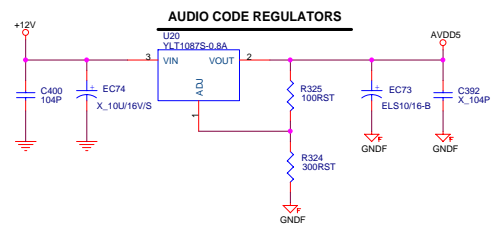
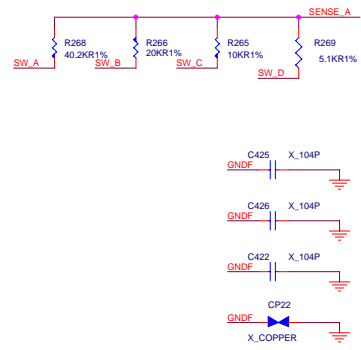
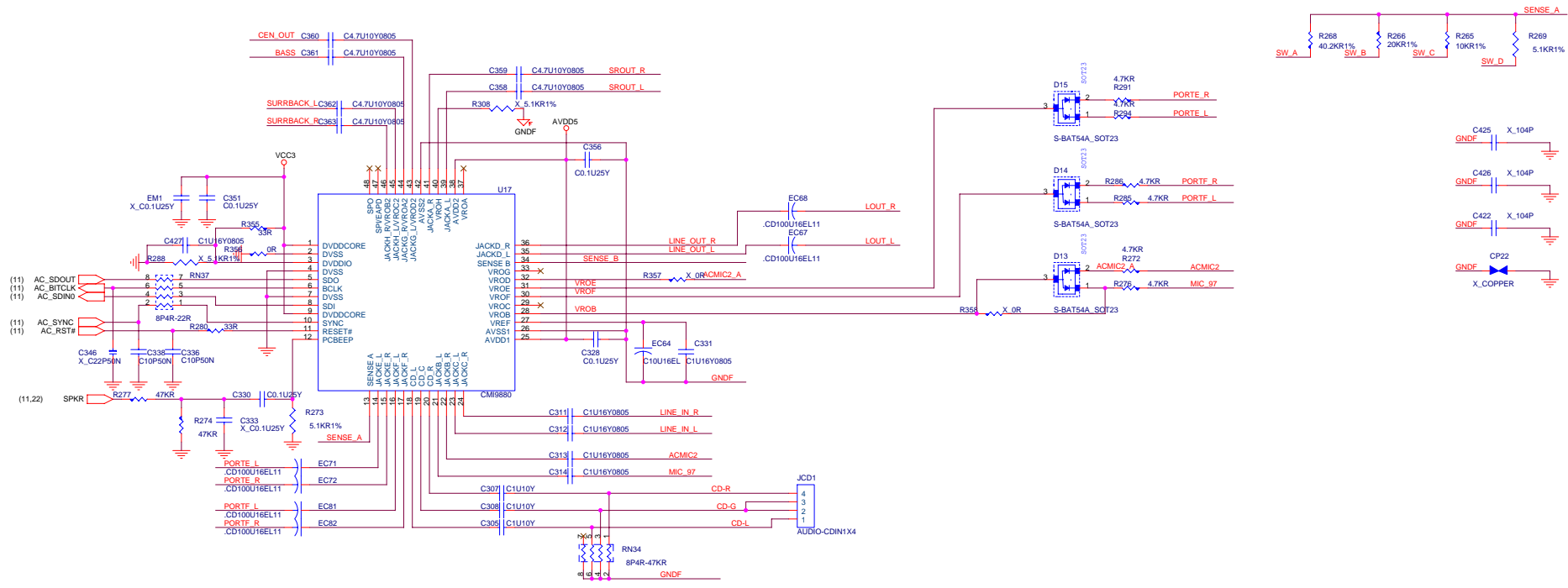
**MICRO-STAR IN'L CO., LTD.**

Title: **CY28416 & FWH**

Size: Document Number **MS-7066** Rev 0B

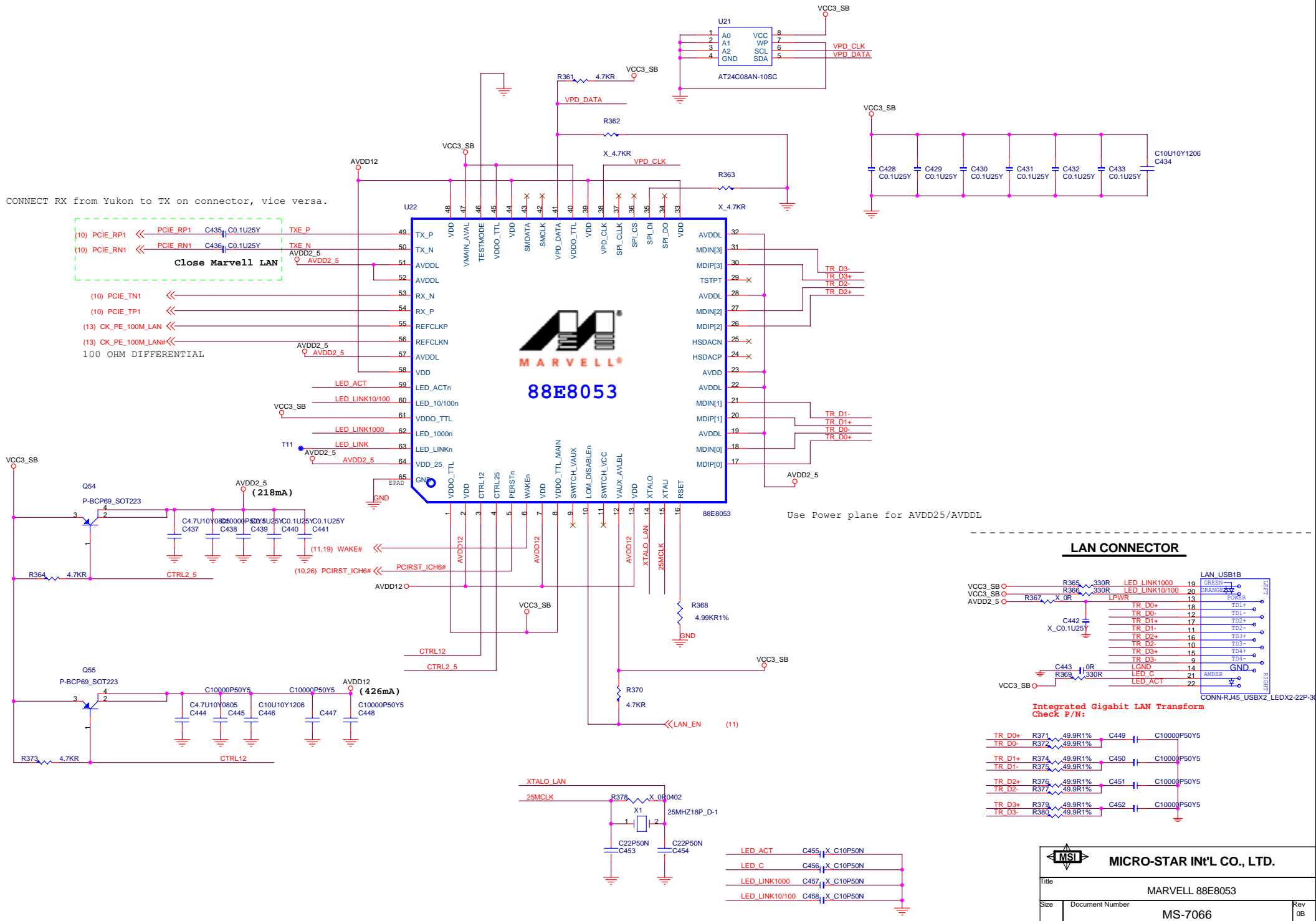
Date: Friday, July 02, 2004 Sheet 13 of 30



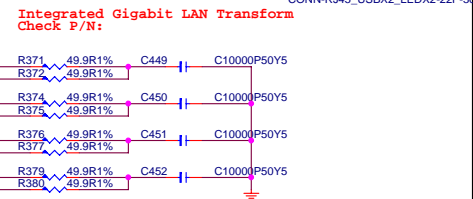
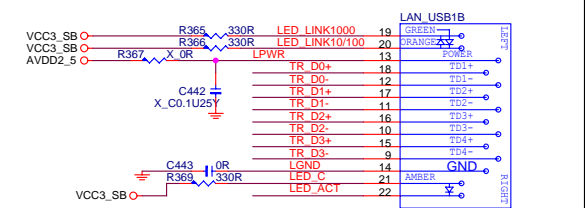


Micro Star Restricted Secret		
Title	Azalia CMI 9880	Rev
Document Number	MS-7066	0B
MICRO-STAR INT'L No. 68, Sec. 4, De St. Jung-Ho City, Taipei Hsien, Taiwan	http://www.msi.com.tw	Last Revision Date: Friday, July 02, 2004 Sheet 15 of 30

CONNECT RX from Yukon to TX on connector, vice versa.



**LAN CONNECTOR**



**MSI MICRO-STAR INT'L CO., LTD.**

Title: MARVELL 88E8053

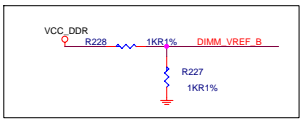
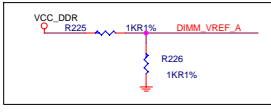
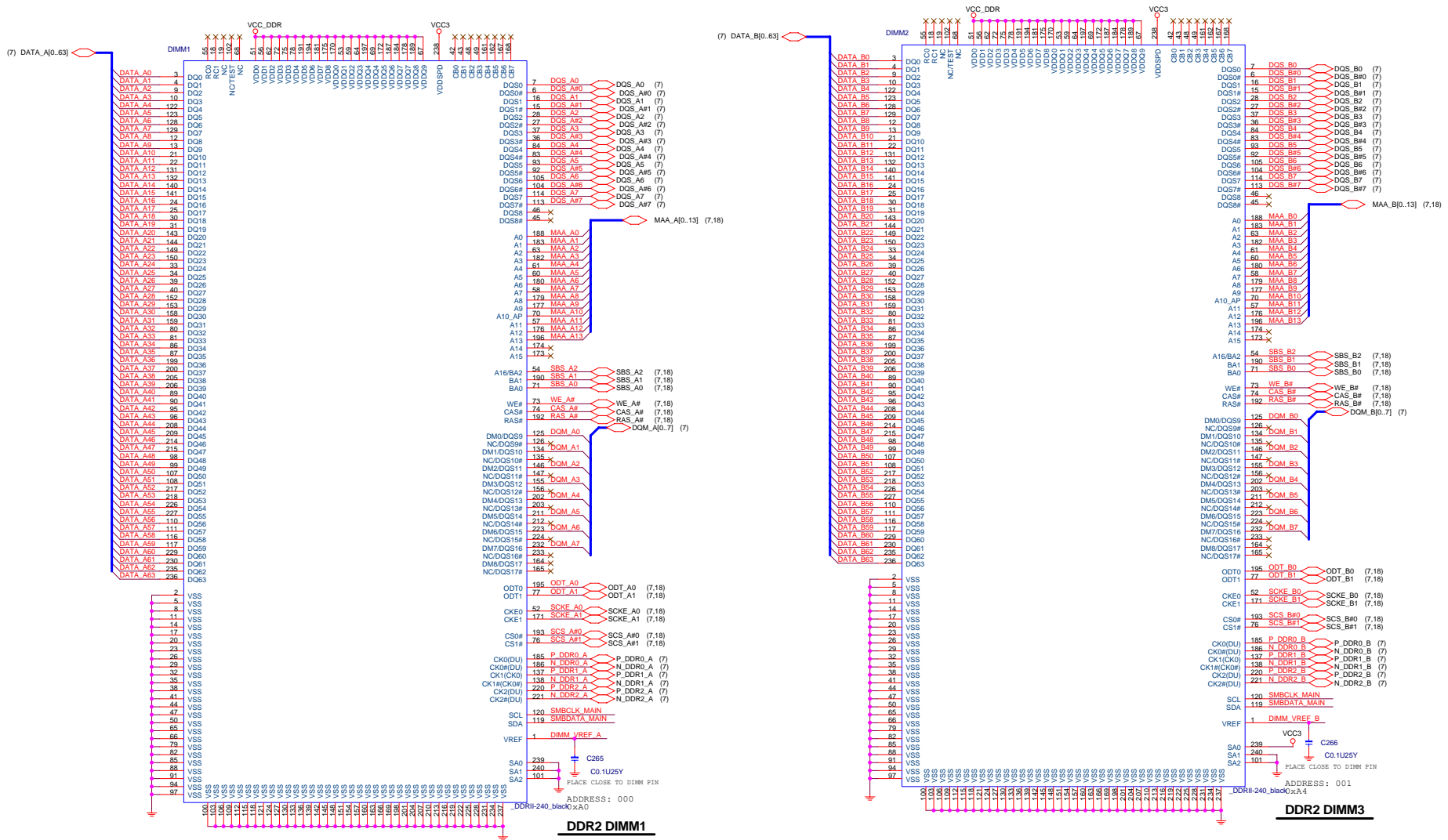
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Date: Friday, July 02, 2004 Sheet 16 of 30



**88E8053**

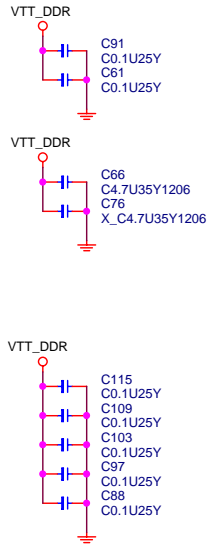




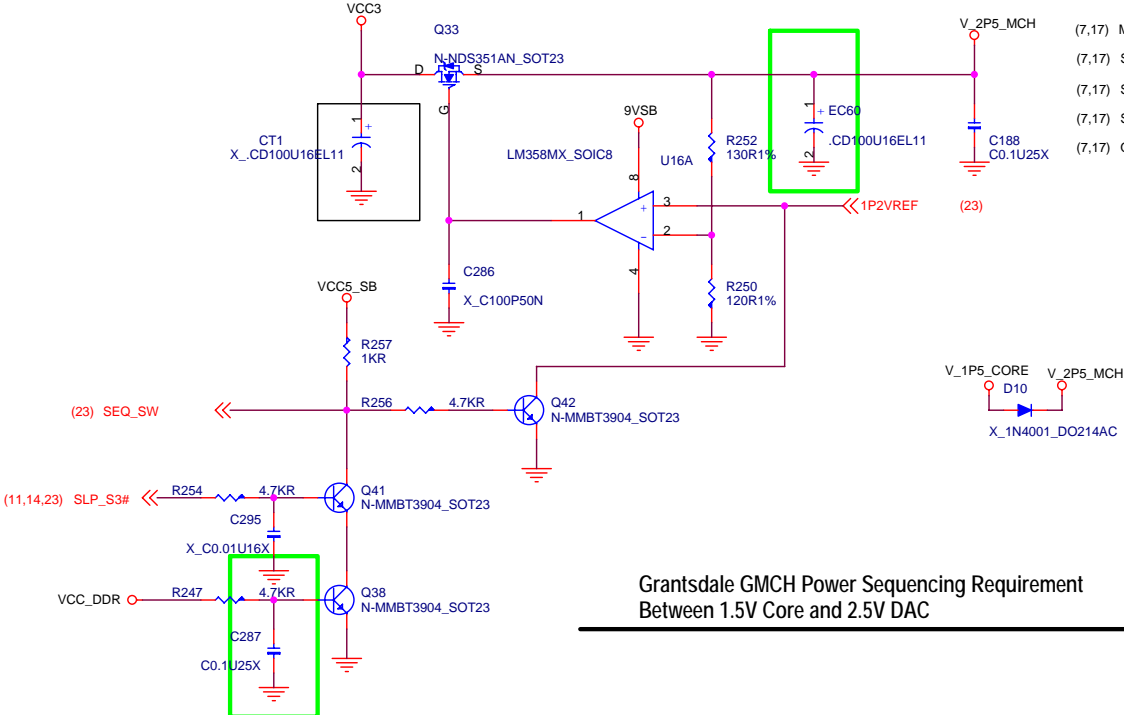
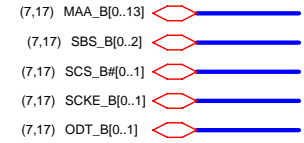
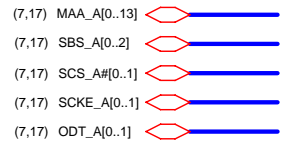
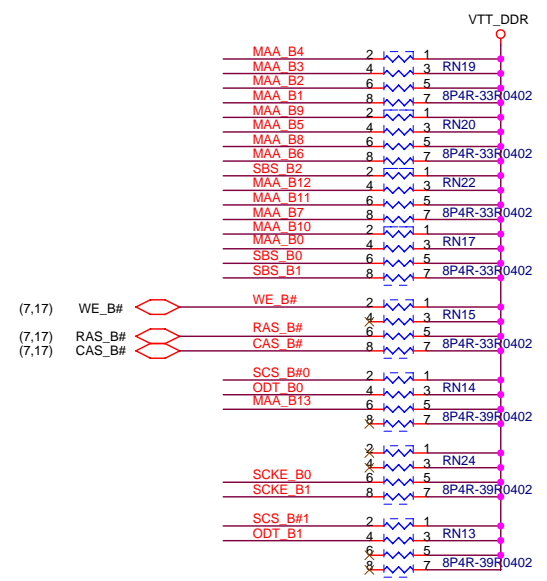
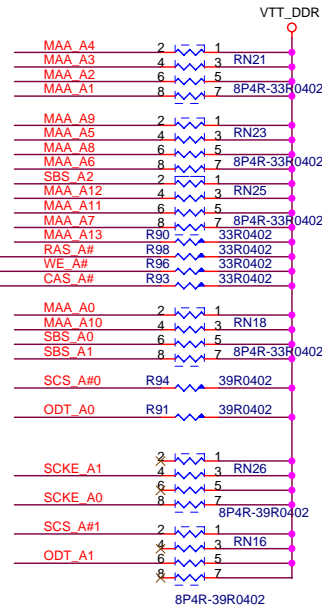
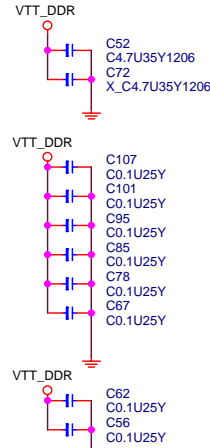
**DDR2 DIMM3**



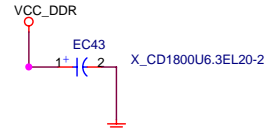
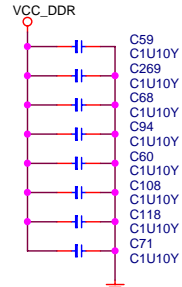
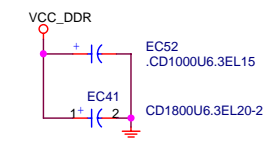
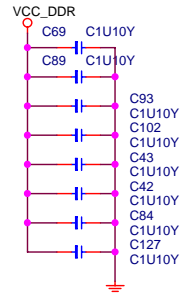
CHANNEL A V\_SM\_VTT DECOUPLING CAPS



CHANNEL B V\_SM\_VTT DECOUPLING CAPS



Grantsdale GMCH Power Sequencing Requirement Between 1.5V Core and 2.5V DAC

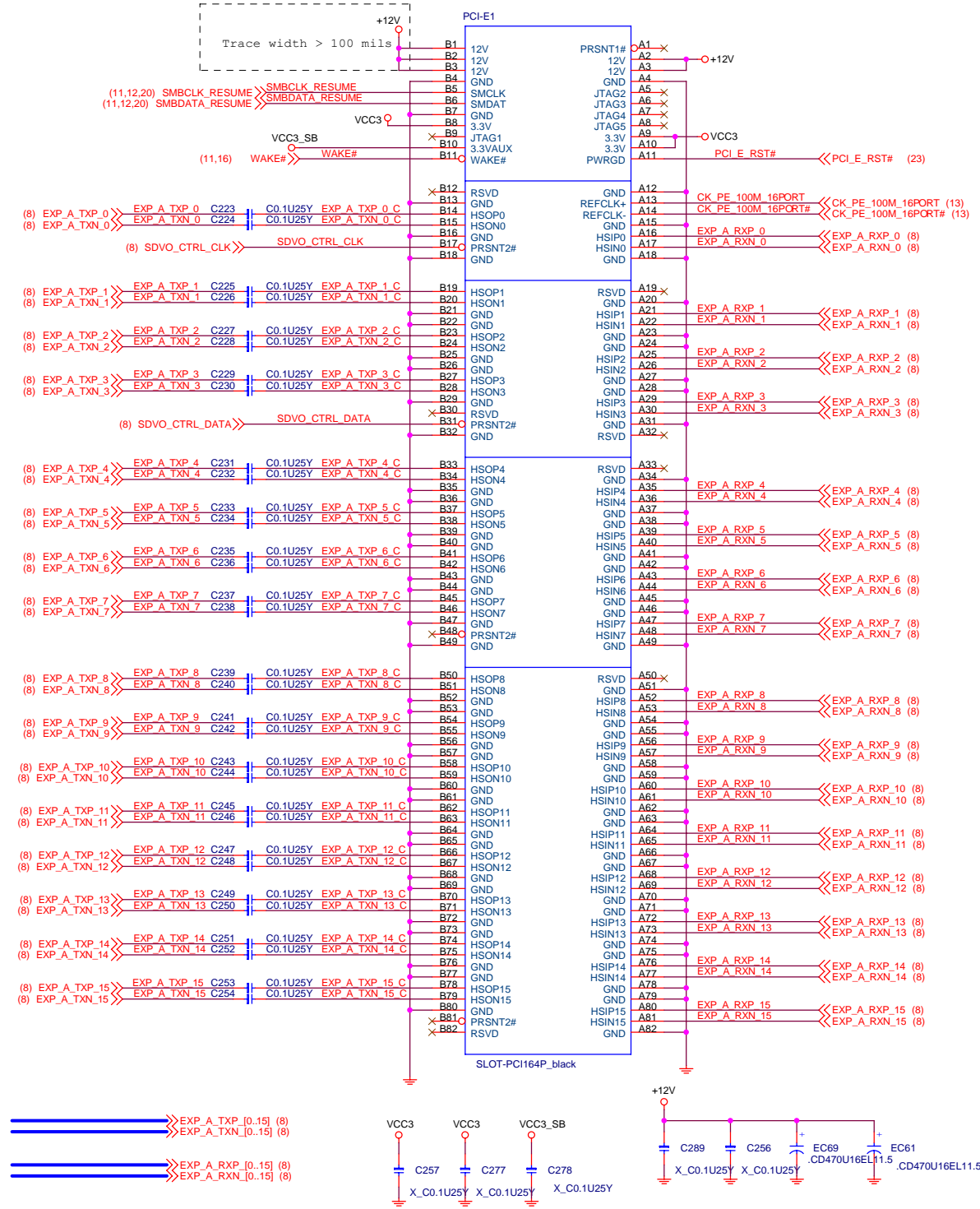


**MSI** MICRO-STAR IN'L CO., LTD.

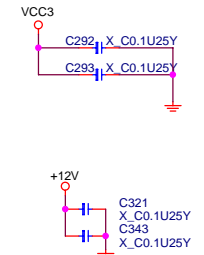
Title: **DDR TERMINATION & VTT DECOUPLING&2.5VDAC**

Size: Document Number **MS-7066** Rev 0B

Date: Friday, July 02, 2004 Sheet 18 of 30



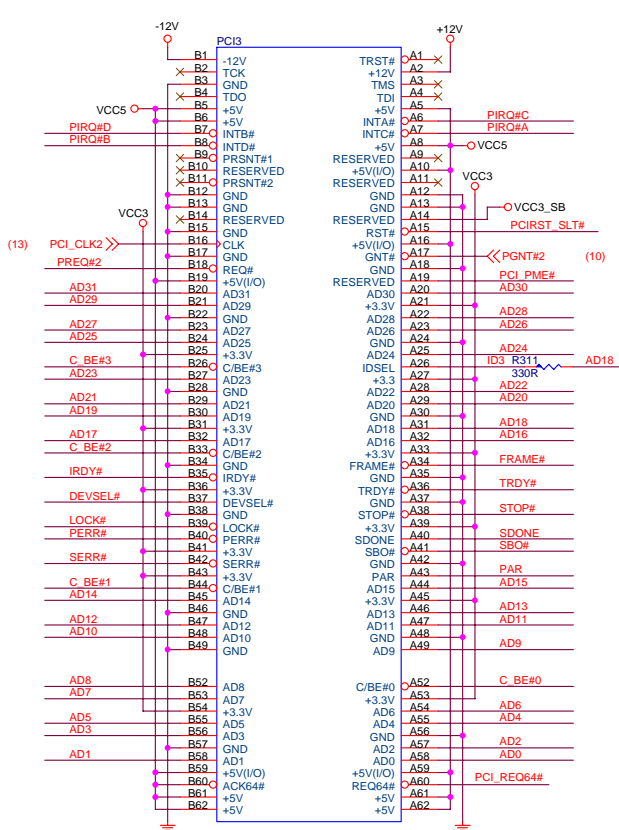
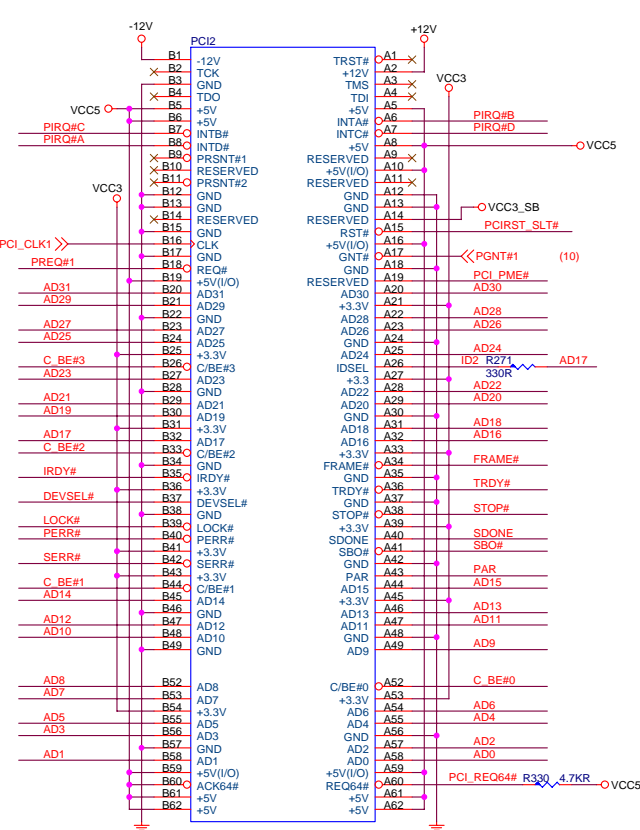
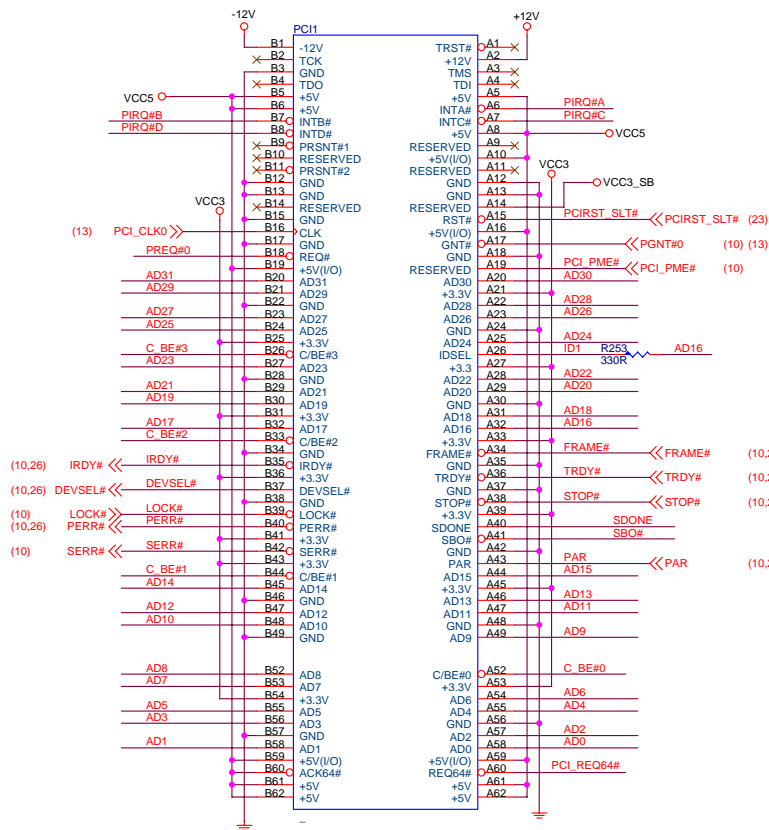
**PCI EXPRESS 1-PORT**



		<b>MICRO-STAR IN'L CO., LTD.</b>	
Title PCI EXPRESS 16 PORT			
Size	Document Number	MS-7066	
Date:	Friday, July 02, 2004	Sheet	19 of 30

**PCI SLOT 1 (PCI VER: 2.2 COMPLY)**

**PCI SLOT 2 (PCI VER: 2.2 COMPLY)**

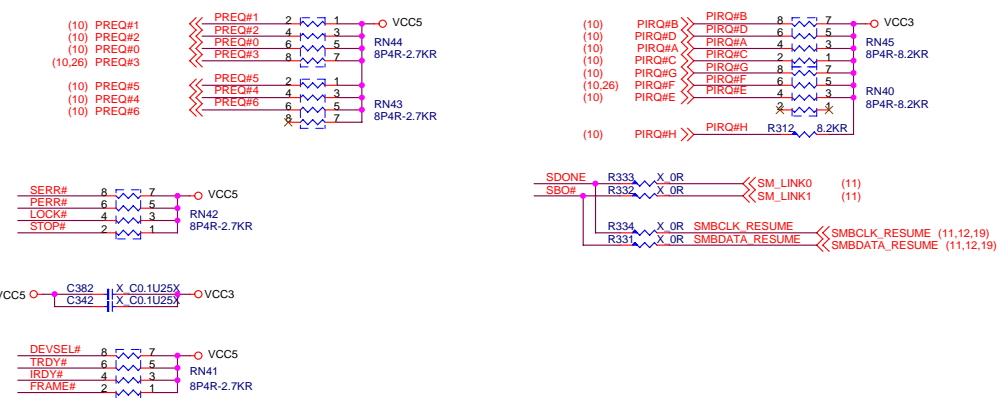


ISDEL = AD16  
 MASTER = PREQ#0  
 PIRQ#A

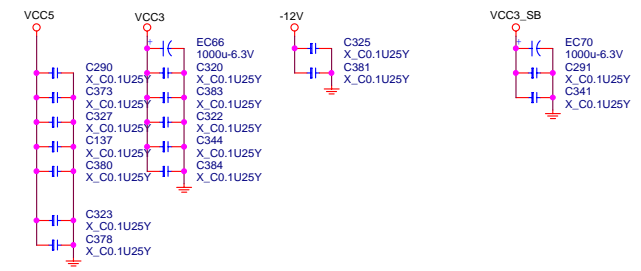
ISDEL = AD17  
 MASTER = PREQ#1  
 PIRQ#B

ISDEL = AD18  
 MASTER = PREQ#2  
 PIRQ#C

**PCI PULL-UP / DOWN RESISTORS**

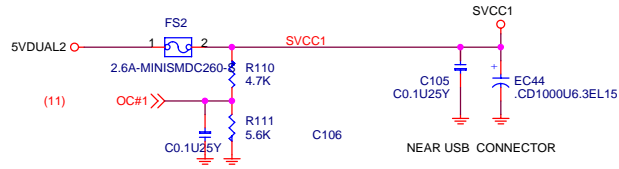


**PCI SLOT DECOUPLING CAPACITORS**



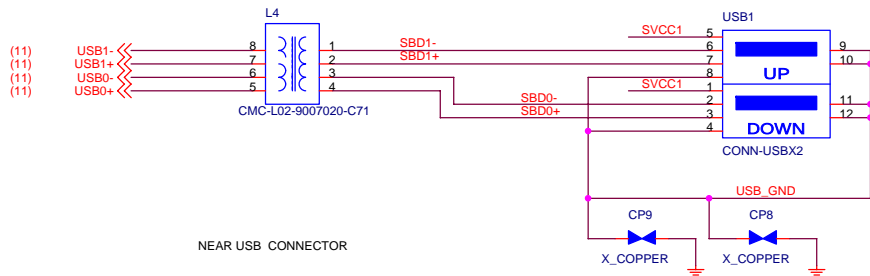
		<b>MICRO-STAR INT'L CO., LTD.</b>	
Title PCI 1 & 2 Slots			
Size	Document Number	MS-7066	
Date:	Friday, July 02, 2004	Sheet	20 of 30

## POWER CIRCUIT FOR USB PORT 0,1,2,3 (REAR)

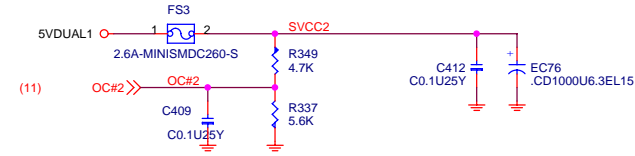


### REAR PANEL USB CONNECTOR FOR USB PORT 0,1

USB Interface  
 Diff. Trace width 7.5 mils & 7.5 mils space.  
 Diff. & other space 20 mils.  
 Length matching: < 150 mils  
 Ttrace length 0" to 17"

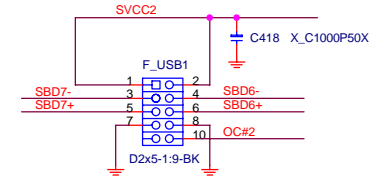
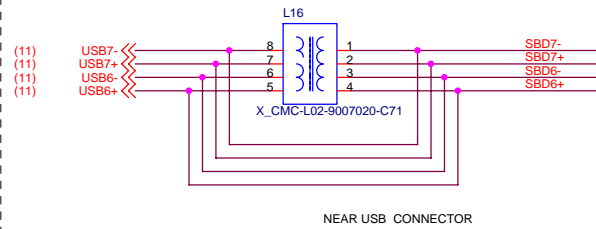


## POWER CIRCUIT FOR USB PORT 4,5,6,7 (FRONT)

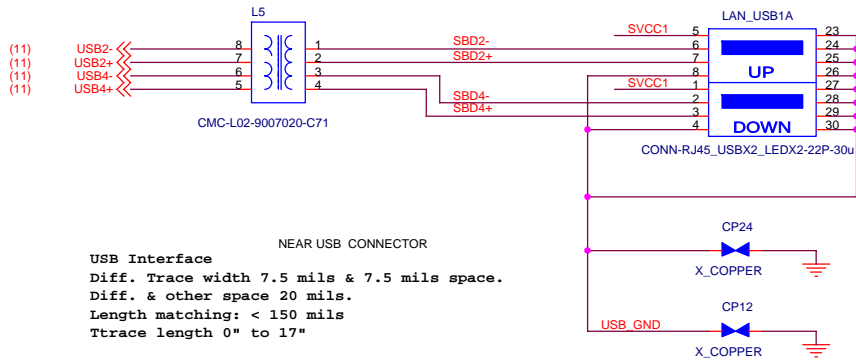


### FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

USB Interface  
 Diff. Trace width 7.5 mils & 7.5 mils space.  
 Diff. & other space 20 mils.  
 Length matching: < 150 mils  
 Ttrace length 0" to 17"

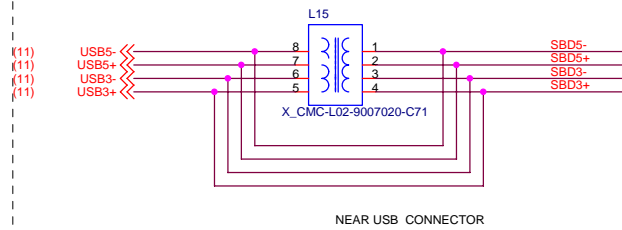


### REAR PANEL USB CONNECTOR FOR USB PORT 2,3

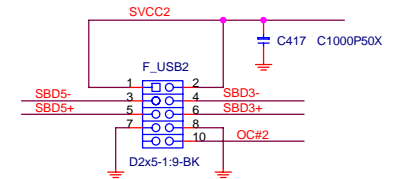


USB Interface  
 Diff. Trace width 7.5 mils & 7.5 mils space.  
 Diff. & other space 20 mils.  
 Length matching: < 150 mils  
 Ttrace length 0" to 17"

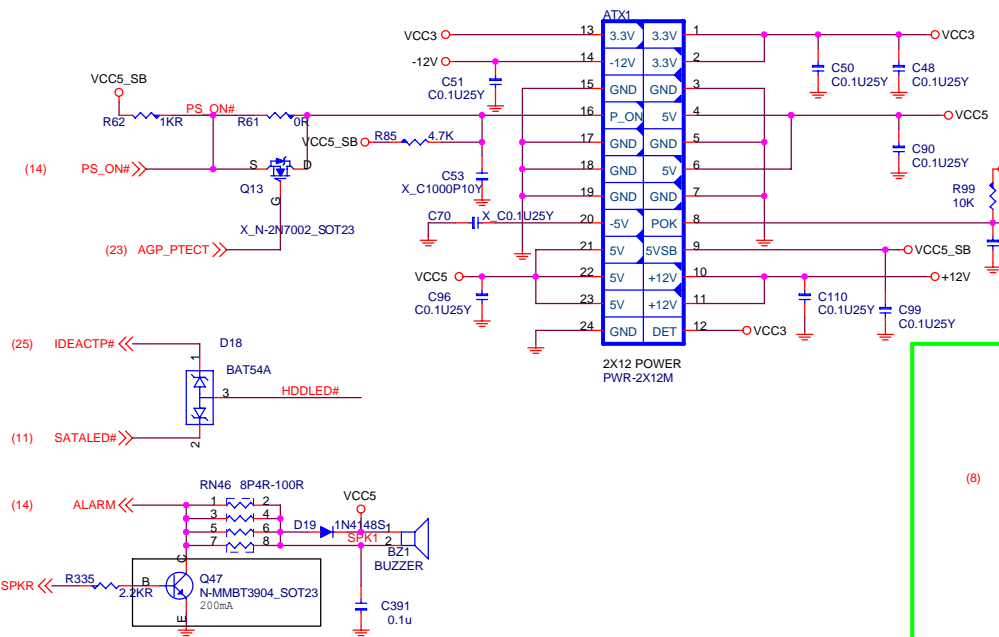
### FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



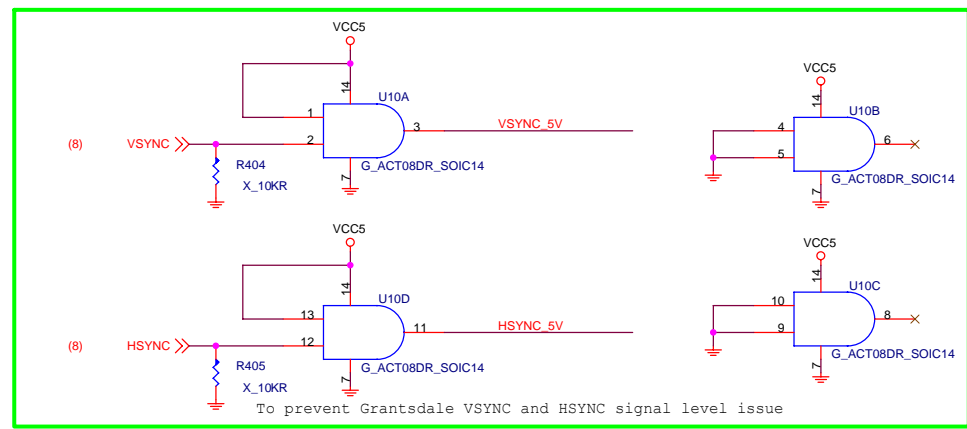
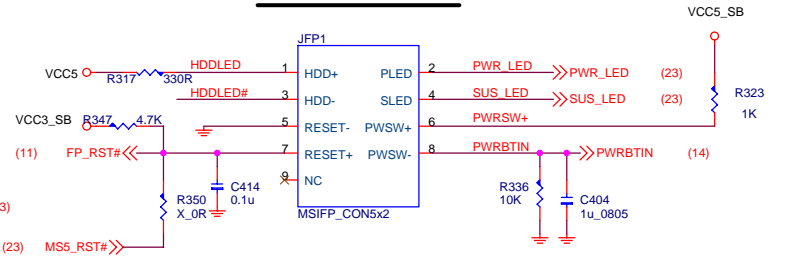
USB Interface  
 Diff. Trace width 7.5 mils & 7.5 mils space.  
 Diff. & other space 20 mils.  
 Length matching: < 150 mils  
 Ttrace length 0" to 17"



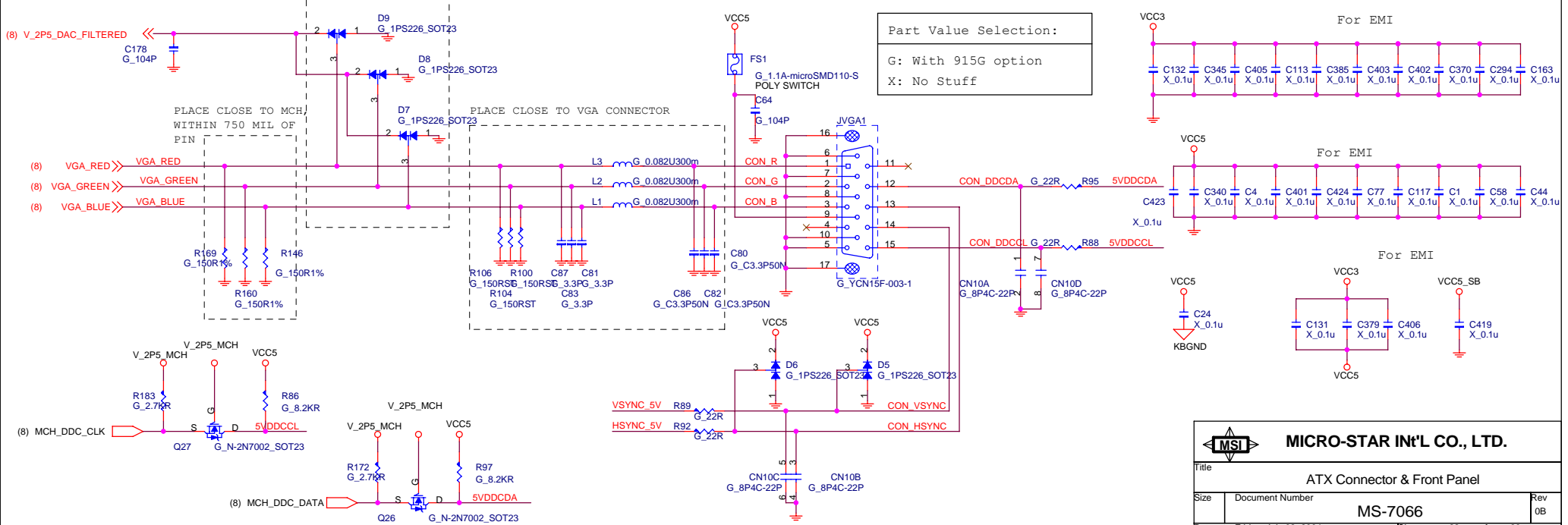
# ATX Connector



# Intel Front Panel



# Video Connector



Part Value Selection:	
G:	With 915G option
X:	No Stuff

**MSI MICRO-STAR IN'L CO., LTD.**

Title: **ATX Connector & Front Panel**

Size: Document Number **MS-7066** Rev 0B

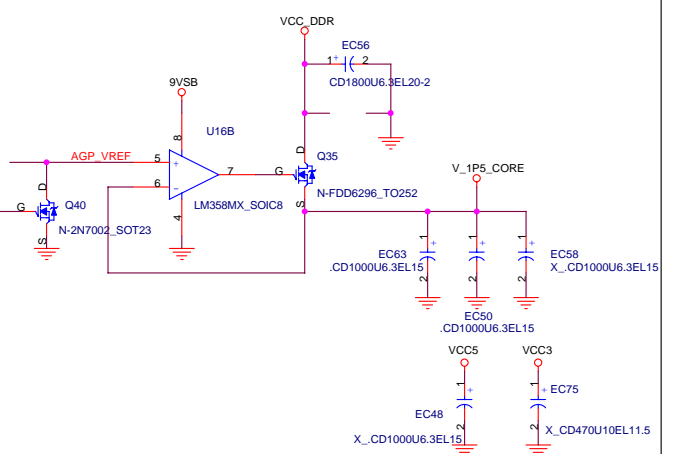
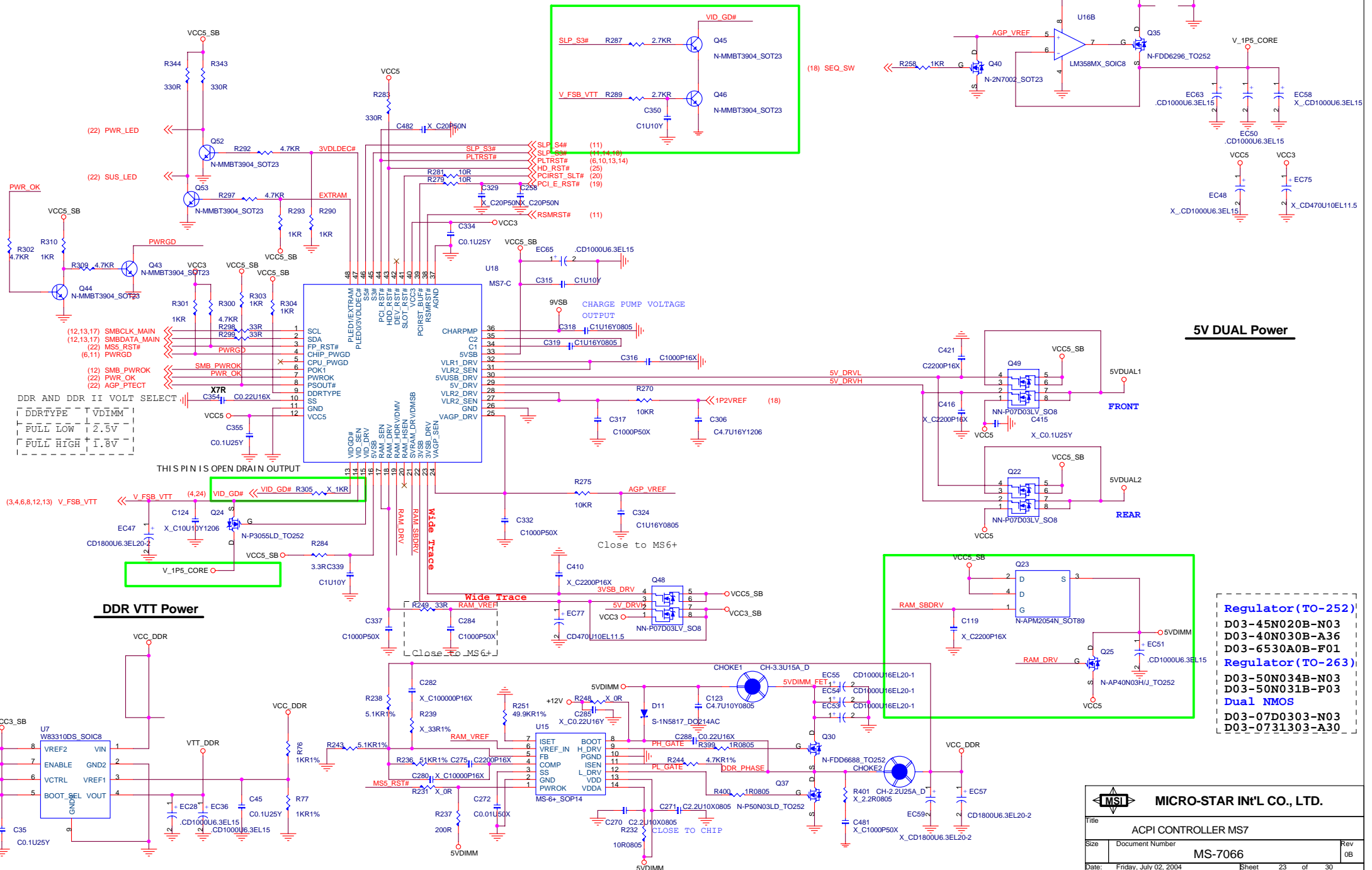
Date: Friday, July 02, 2004 Sheet 22 of 30

# ACPI Controller

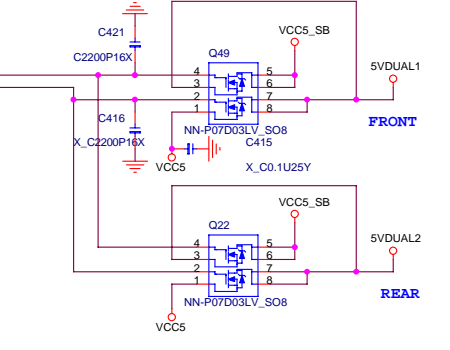
**3VSB MODE SELECT**  
3VSB MODE SELECT  
SINGLE MOSFET FULL HIGH  
DUAL MOSFET FULL LOW

**VDIMM LINEAR OR PWM SELECT**  
VDIMM MODE SELECT  
LINEAR REGULATOR PULL LOW  
PWM REGULATOR PULL HIGH

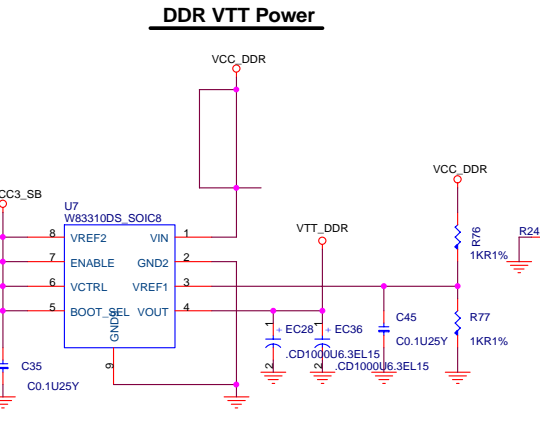
## PCI-Express POWER



## 5V DUAL Power



- Regulator (TO-252)  
D03-45N020B-N03  
D03-40N030B-A36  
D03-6530A0B-F01
- Regulator (TO-263)  
D03-50N034B-N03  
D03-50N031B-P03
- Dual NMOS  
D03-07D0303-N03  
D03-0731303-A30

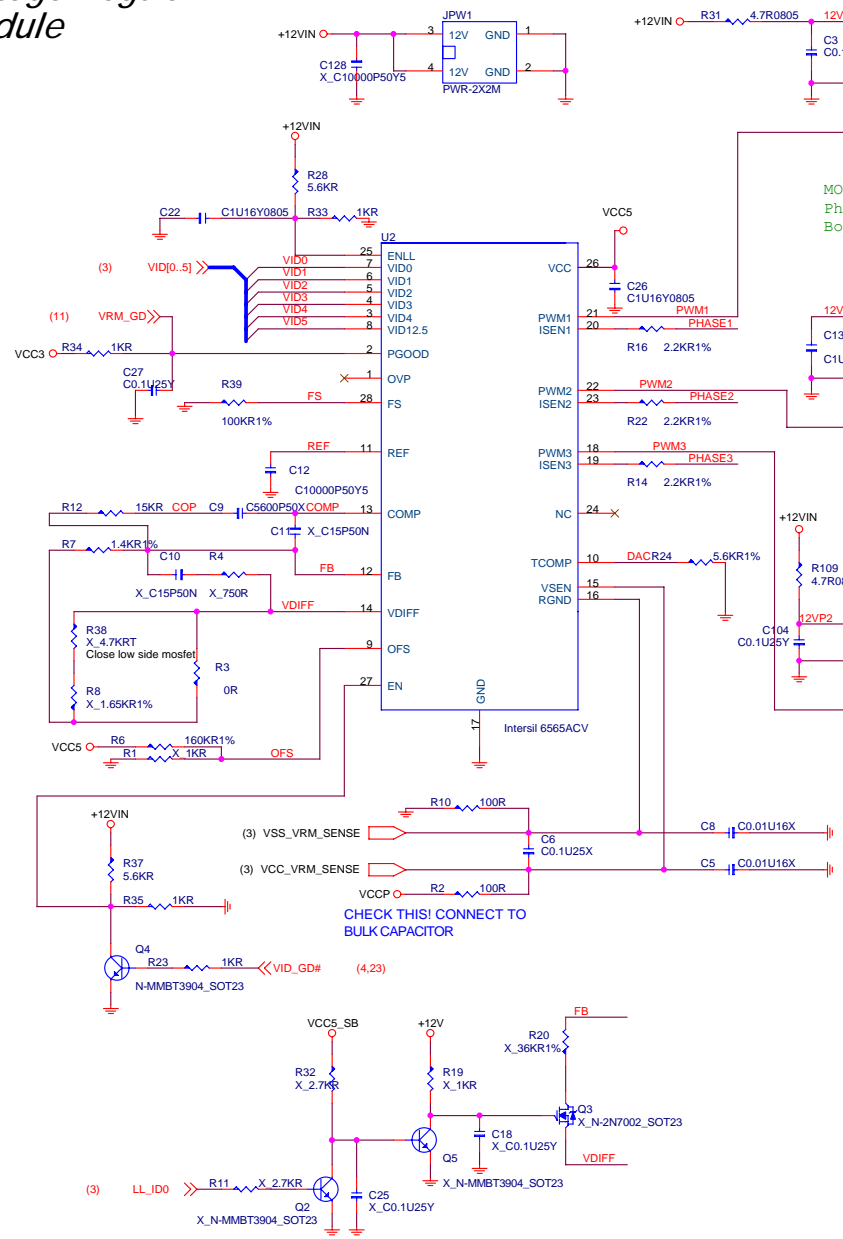


MICRO-STAR INT'L CO., LTD.		
Title: ACPI CONTROLLER MS7		
Size: 23	Document Number: MS-7066	Rev: 0B
Date: Friday, July 02, 2004		
Sheet 23 of 30		

# Voltage Regular Module

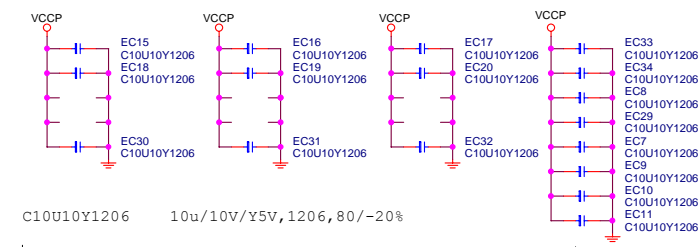
IPF06N03LA Rds (on)=8.7mΩ (@4.5V, 30A), Vgs (on)=1.2~2V, Id=50A, Ciss=3110pF, Qg=10nC, Vds=25V, Vgs=±20V  
 C100U2SP ESR<13mΩ, Ripple cur.<2.7A, LC<12uA, 105C  
 .CD3300U6.3EL25 ESR<12mΩ, Ripple cur.<2800mA, 105C, longlife3000hrs, KZG Series  
 560u\_2.5V ESR=6mΩ, Ripple cur.=4400mA, Lc.<500uA, 105C/2000hrs  
 1800UF/6.3V ESR<12mΩ, Ripple cur.<2350mA, 105C, longlife change from 2000hrs to 3000hrs, KZJ series  
 0.6uH/40A 0.6u/20%, Isat=40A, Rdc=1.2m ohm, PEW wire  
 CH-1.2U18A 1.2u/20%, Dip-2/vertical 17.5mm, 1.2ψ/5.5turns, 18A

TDP = 115 W  
 VR\_TDC = 101 A  
 Icc(max) = 119 A  
 Tejas Tcase = [P x 0.213] + 43.3  
 Prescott Tcase = [P x 0.25] + 43.3



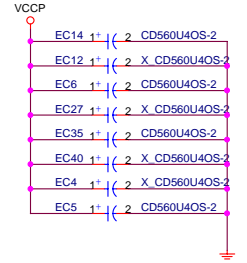
MOSFET Gate signal : 20 mils  
 Phase signal : 20 mils  
 Boot signal : 16 mils

## CPU DECOUPLING CAPACITORS

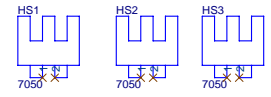


Place these caps within socket cavity

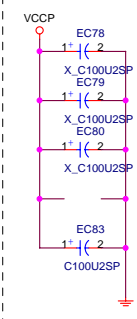
## OS-CON Capacitors



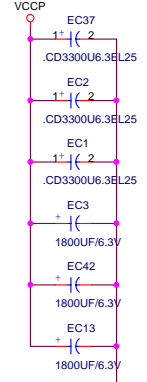
## MOSFET Heatsinks



## SP Capacitors



## EL Capacitors

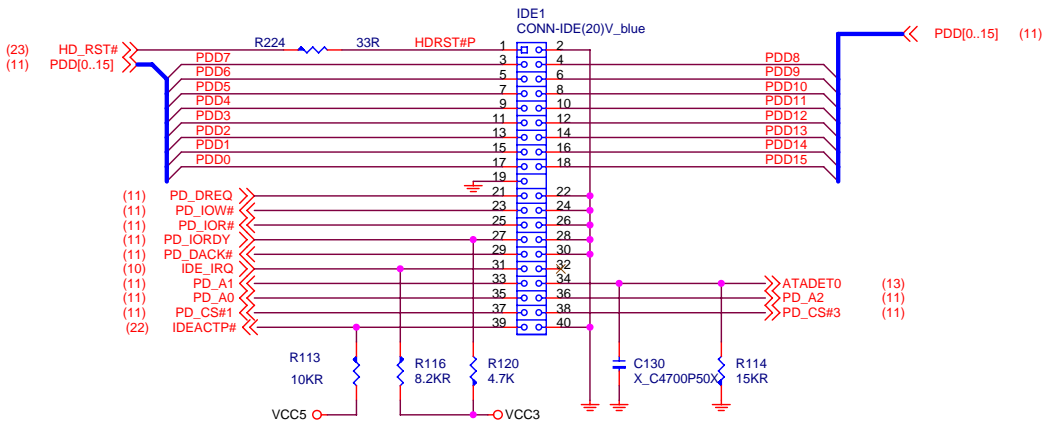


Solder Side

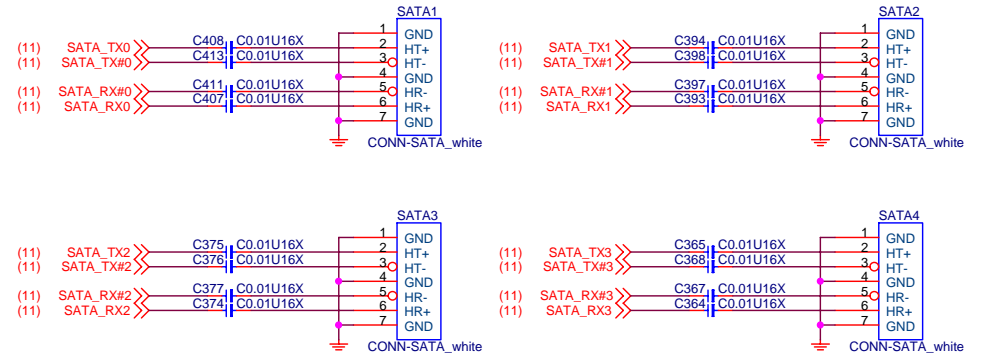
<b>MICRO-STAR IN'L CO., LTD.</b>			
Title VRM 10.1 - Intersil 6565ACV 3 Phase			
Size	Document Number	MS-7066	
Date:	Friday, July 02, 2004	Sheet	24 of 30



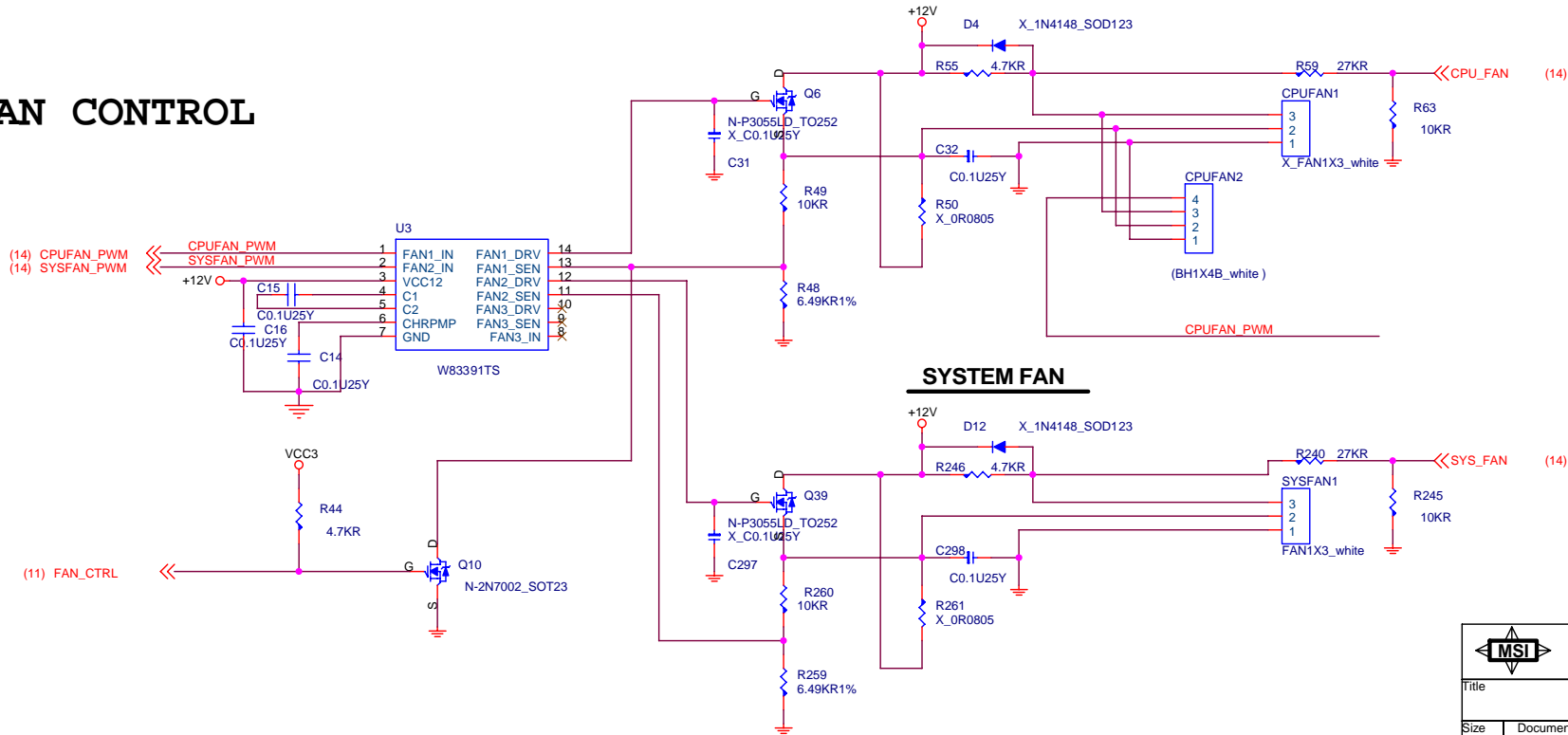
### ATA 33/66/100 IDE Connectors




### SERIAL ATA CONNECTOR BLOCK



### FAN CONTROL

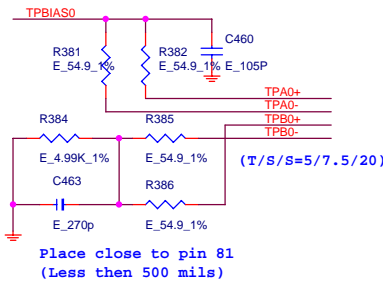
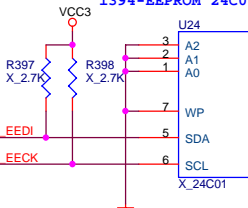
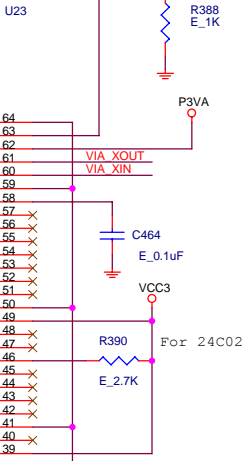
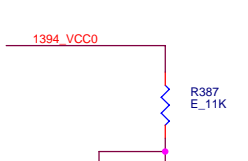
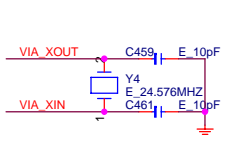
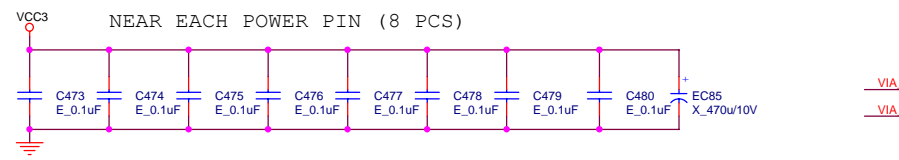
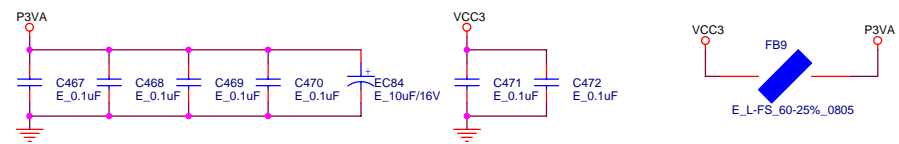
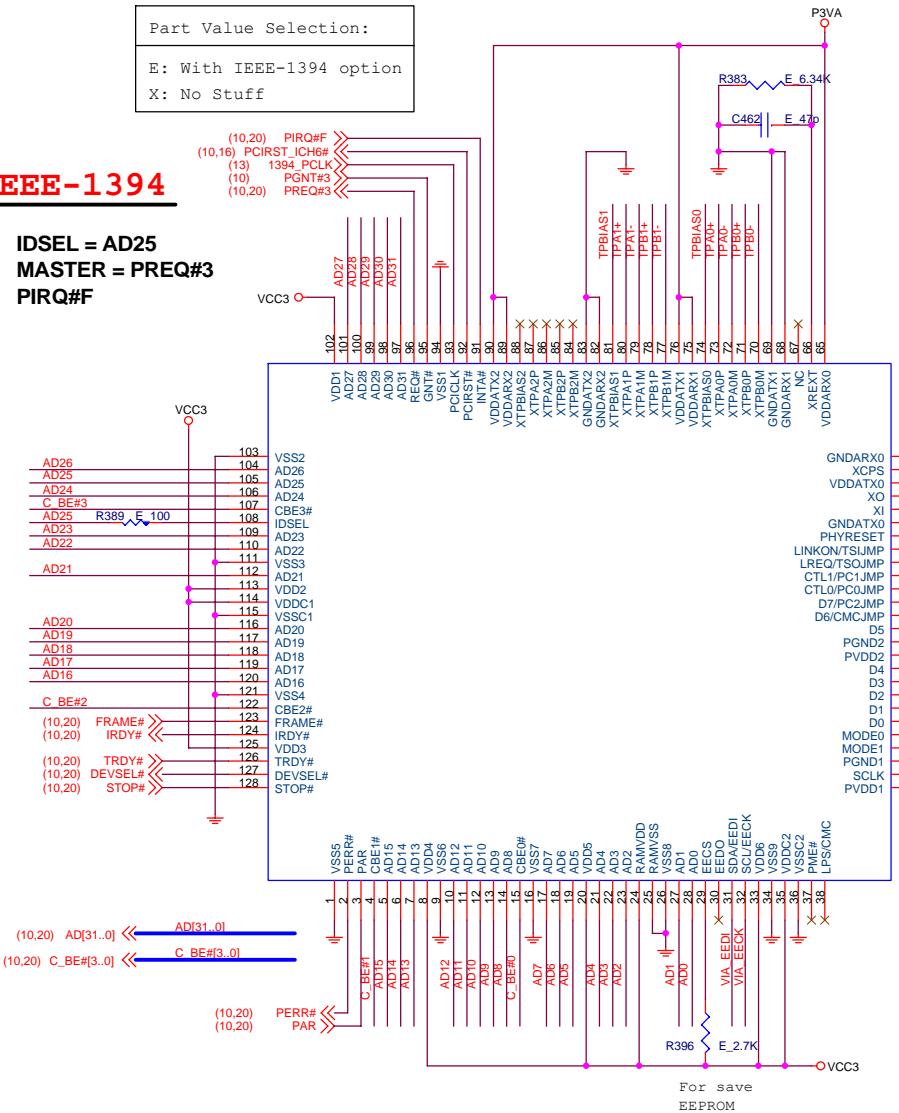


 <b>MICRO-STAR INT'L CO., LTD.</b>		
Title: FAN & IDE Connectors		
Size	Document Number	Rev
	MS-7066	0B
Date:	Friday, July 02, 2004	Sheet 25 of 30

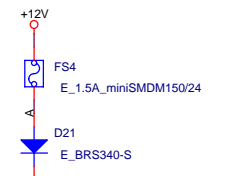
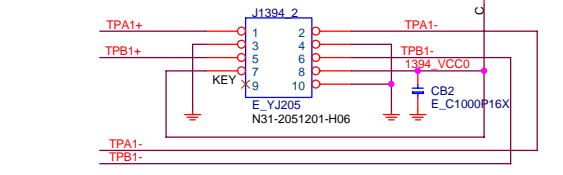
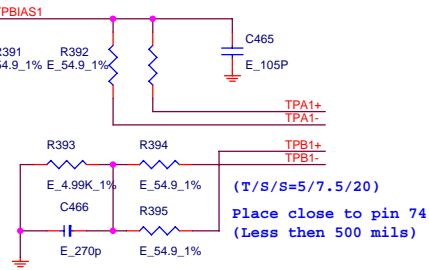
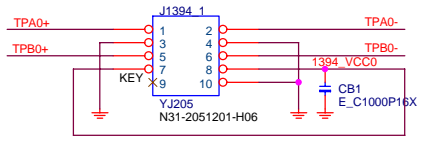
Part Value Selection:  
 E: With IEEE-1394 option  
 X: No Stuff

# IEEE-1394

**IDSEL = AD25**  
**MASTER = PREQ#3**  
**PIRQ#F**



## FRONT 1394 PORT



TC = 0-55°C, VCC = 3.3V/+10%, GND = 0V					
Symbol	Parameter	Typ	Max	Unit	Condition
ECC	Power Supply Current-VCC	89	107	mA	S400, two ports transmitting

**MSI**  
 Link to our factory

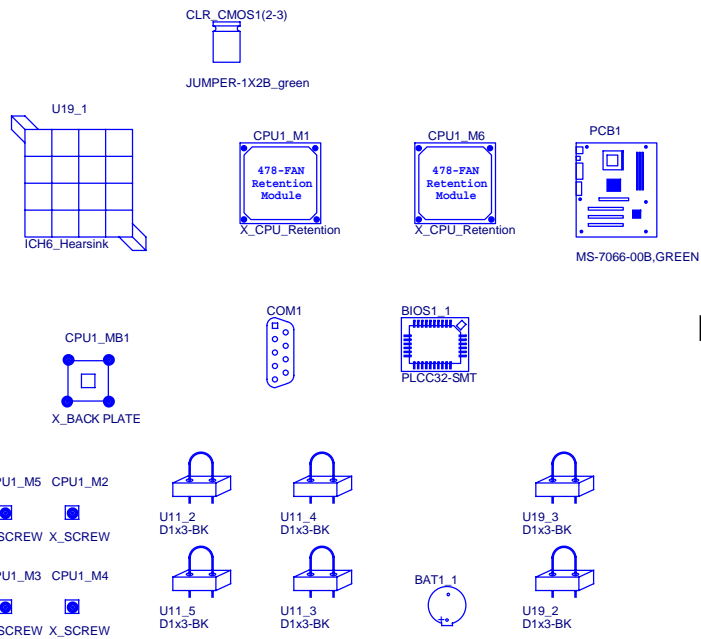
**MICRO-START INT'L CO.,LTD.**

Title: **VIA-6307 IEEE1394 Controller**

Size	Document Number	Rev
A3	<b>MS-7066</b>	<b>0B</b>

Date: Friday, July 02, 2004 Sheet 26 of 30

## MANUAL PART



Model option table

Model type	Function	BOM Config	ERP BOM No.
MS7066	915G+ICH6+G-bit Lan+1394	Cfg7066-00B-SIG	601-7066-XXX
MS7066	915P+ICH6+G-bit Lan+1394	Cfg7066-00B-SID	

**ICH6**

GPIO	Alt Func	Pin	I/O/NC	Power	PU	SMI	Tol	Default	Rickles Signal Name
GPI[0]	PCIREQ[6]#	B7	I	V5REF	N	Y	5)	N/A	PREQ#6
GPI[1]	PCIREQ[5]#	E8	I	V5REF	N	Y	5	N/A	PREQ#5
GPI[2]	PIRQE#	D9	I	V5REF	N	Y	5	N/A	PIRQ#E
GPI[3]	PIRQF#	C7	I	V5REF	N	Y	5	N/A	PIRQ#F
GPI[4]	PIRQG#	C6	I	V5REF	N	Y	5	N/A	PIRQ#G
GPI[5]	PIRQH#	M3	I	V5REF	N	Y	5	N/A	PIRQ#H
GPI[6]	unmuxed	AD19	I	Vcc3p3	N	Y	3.3	N/A	strapped hi
GPI[7]	unmuxed	AE19	I	Vcc3p3	N	Y	3.3	N/A	NC
GPI[8]	unmuxed	R1	I	VccSus3p3	N	Y	3.3	N/A	NC
GPI[9]	OC[4]#	C23	I	VccSus3p3	N	Y	3.3	N/A	OC#2
GPI[10]	OC[5]#	D23	I	VccSus3p3	N	Y	3.3	N/A	OC#2
GPI[11]	SMBALERT#	W6	I	VccSus3p3	N	Y	3.3	N/A	SMB ALERT#
GPI[12]	unmuxed	M2	I	Vcc3p3	N	Y	3.3	N/A	NC
GPI[13]	unmuxed	R6	I	VccSus3p3	N	Y	3.3	N/A	strapped hi / SIO PME#
GPI[14]	OC[6]#	C25	I	VccSus3p3	N	Y	3.3	N/A	OC#2
GPI[15]	OC[7]#	C24	I	VccSus3p3	N	Y	3.3	N/A	OC#2
GPO[16]	PCIGNT[6]#	D8	O	Vcc3p3	U	N	3.3	1	NC
GPO[17]	PCIGNT[5]#	F6	O	Vcc3p3	U	N	3.3	1	PGNT#5
GPO[18]	blink	AC21	O	Vcc3p3	N	N	3.3	1	NC
GPO[19]	blink	AB21	O	Vcc3p3	N	N	3.3	1	GPO BIOS WP#
GPO[20]	unmuxed	AD22	O	Vcc3p3	N	N	3.3	1	GPO FAN CTRL
GPO[21]	unmuxed	AD20	O	Vcc3p3	N	N	3.3	1	NC
GPO[23]	unmuxed	AD21	O	Vcc3p3	N	N	3.3	0	NC
GPIO[24]	unmuxed	V3	I/O	VccSus3p3	N	N	3.3	Out-1	NC
GPIO[25]	Internal 2.5V	p5	I/O	VccSus3p3	D	N	3.3	Out-1	strapped low for 2.5v reg internal
GPI[26]	SATA[0]GP	AF17	I	Vcc3p3	N	N	3.3	N/A	~GPI VGA CABLE DET/strapped hi
GPIO[27]	unmuxed	R3	I/O	VccSus3p3	N	N	3.3	Out-1	NC
GPIO[28]	unmuxed	T3	I/O	VccSus3p3	N	N	3.3	Out-1	GPO LAN EN
GPI[29]	SATA[1]GP	AE18	I	Vcc3p3	N	N	3.3		ICH GPI29/strapped hi
GPI[30]	SATA[2]GP	AF18	I	Vcc3p3	N	N	3.3		ICH GPI30/strapped hi
GPI[31]	SATA[3]GP	AG18	I	Vcc3p3	N	N	3.3		ICH GPI31/strapped hi
GPIO[32]	unmuxed	AF19	I/O	Vcc3p3	N	N	3.3	Out-1	NC
GPIO[33]	unmuxed	AF20	I/O	Vcc3p3	N	N	3.3	Out-1	NC
GPIO[34]	unmuxed	AC18	I/O	Vcc3p3	N	N	3.3	Out-1	NC
GPIO[40]	REQ4#	F7	I	V5REF	N	N	5		NC
GPIO[41]	LDRQ1#	P4	I	Vcc3p3	U	N	3.3		NC
GPIO[48]	GNT4#	E7	O	Vcc3p3	N	N	3.3		NC
GPIO[49]	CPUPWRGD	AG25	OD	V CPU IO	N	N	3.3		H PWRGD

Note: All inputs are sticky. The status bit remains set as long as the input was asserted for two clocks. GPI's are sampled on PCI clocks in S0/S1. GPIs are sampled on RTC clocks in S3/S4/S5.

**FWH** Note: FWH GPs should only be used for static options, do not put dynamic nets on these

GPIO	Pin#	Power	Tol	Signal Name
FPGI[0]	6	Main	3.3	ATADET0
FPGI[1]	5	Main	3.3	pull-down
FPGI[2]	4	Main	3.3	pull-down
FPGI[3]	3	Main	3.3	pull-down
FPGI[4]	30	Main	3.3	pull-down

**PCI Config.**

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIROA PIROB PIROC PIROD	PCI_REQ#0 PCI_GNT#0	AD16	PCICLK0
PCI Slot 2	PIROB PIROC PIROD PIROA	PCI_REQ#1 PCI_GNT#1	AD17	PCICLK1
PCI Slot 3	PIROC PIROD PIROA PIROB	PCI_REQ#2 PCI_GNT#2	AD18	PCICLK2
1394	PIROF	PCI_REQ#3 PCI_GNT#3	AD25	1394_PCLK

**DDRII DIMM Config.**

DEVICE	ADDRESS	CLOCK
DIMM 1	A0H	MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2
DIMM 2	A2H	MCLK_B0/MCLK_B#0 MCLK_B1/MCLK_B#1 MCLK_B2/MCLK_B#2

**JUMPER SETTING**

<b>RTCST</b>	(1-2) CLEAR	(2-3) NORMAL
--------------	-------------	--------------

<b>Tejas</b>		
0.8375V - 1.6000V Core	-	95A
1.2V FSB Vtt	-	TBD A

<b>Gransdale GMCH</b>		
1.2V FSB Vtt	-	1.2A
1.8V DDR2 I/O(S0,S1)	-	4.7A
1.8V DDR2 I/O(S3)	-	25mA
*2.5V DAC	-	0.07A
2.5V HV	-	TBD A
1.5V Core (Integrated)	-	9.7A
1.5V Core (Discrete)	-	7.7A
*1.5V PCI Express	-	1.4A

<b>ICH6</b>		
1.2V VCC_CPU	-	TBD A
1.5V Core	-	1.88A
*1.5V PCI Express	-	560mA
1.5V SATA	-	430mA
+3.3V VccSus	-	330mA
RTC (G3)	-	5uA
5VRef	-	TBD A
5VrefSus	-	TBD A
+3.3V	-	180mA

<b>FWH</b>		
+3.3V (S0,S1)	-	107mA

<b>ISL6565</b>		
VCCP	VRM 10.1	
0.8375V-1.6000V	95A	
3-Phase Switch		

<b>W83310DS</b>		
VTT_DDR		
0.9V	Linear	1.5A

<b>MS7 Regulator</b>		
V_FSB_VTT		
1.2V	Linear	5.0A
V_1P5_CORE		
1.5V (S0,S1)	14A	
Linear		
V_2P5_MCH		
2.5V	Linear	100mA
VCC3_SB		
3.3V	Linear	1.5A
5VDUAL1,2		
5V	Linear	22mA

<b>MS6+ Regulator</b>		
VCC_DDR		
1.8V	Switch	20A
Linear (S3)		
		425mA

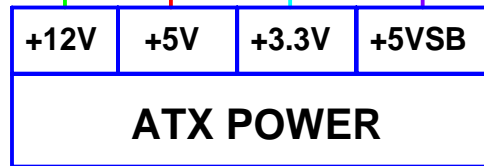
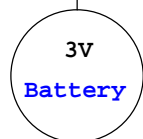
<b>DDR DIMM &amp; TERMINATOR</b>		
0.9V VTT_DDR	-	1.2A
1.8V VCC_DDR (S0,S1)	-	9.4A
1.8V VCC_DDR (S3)	-	400mA

<b>PCI Express x16 slot</b>		
+12V	-	5.5 A
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	3.0A

<b>PCI slot x3</b>		
+3.3Vaux (wake)	-	375mA
+3.3Vaux (no wake)	-	20mA
+3.3V	-	7.6A
+5V	-	5.0A
+12V	-	0.5A

<b>USB</b>		
+5V (S0,S1)	-	4.0A
+5V (S3)	-	20mA

<b>PS2</b>		
+5V (S0,S1)	-	345mA
+5V (S3)	-	2.0mA



03/12

Page 4 add C74, C75 for CPU PLL PWR (ADV suggest)  
Page 10 add PGNT5# and R351 for DEBUG  
Page 23 Del R305 (MS7 time issue )  
Page 22 add R61 del Q13 (AGP\_PTECT not used )  
Page 5 add R72 ,R75 ( referenced MS-7052 )  
Page 3,5 add CPU TEST PIN

03/15

Page 24 Change PWM CHOCK2~4  
Page 6 Add R229ICH\_SYNC# pull high V\_2P5\_MCH referenced MS-7028

03/18

Page 15 Change D13, D14, D15 BAT54A footprint

03/22

Page 8 Del R132 R149 R157 CYPRESS RECOMMEND  
Page 14 Add C40 near Super IO  
Page 23 Del EC59 add EC56 ( 卡件 )

04/27

Page 26 Add VIA-6307 IEEE 1394 Controller  
Page 16 Change PCIE GigaLan from 82570EI to MARVELL 88E8052  
Page 15 Swap AUDIO1 and AUDIO2  
Change COPPER library to NC\_T  
Page 13 Change JLPC1 library  
Page 22 Add 22P at CN10 to meet SPEC.  
Page 21 Add L4 L5 for EMI  
Page 14 Add R402 RN51 ~RN54 for EMI

Title		
HISTORY		
Size	Document Number	Rev
B	MS-7066	0B
Date:	Friday, July 02, 2004	Sheet 30 of 30